EDN®

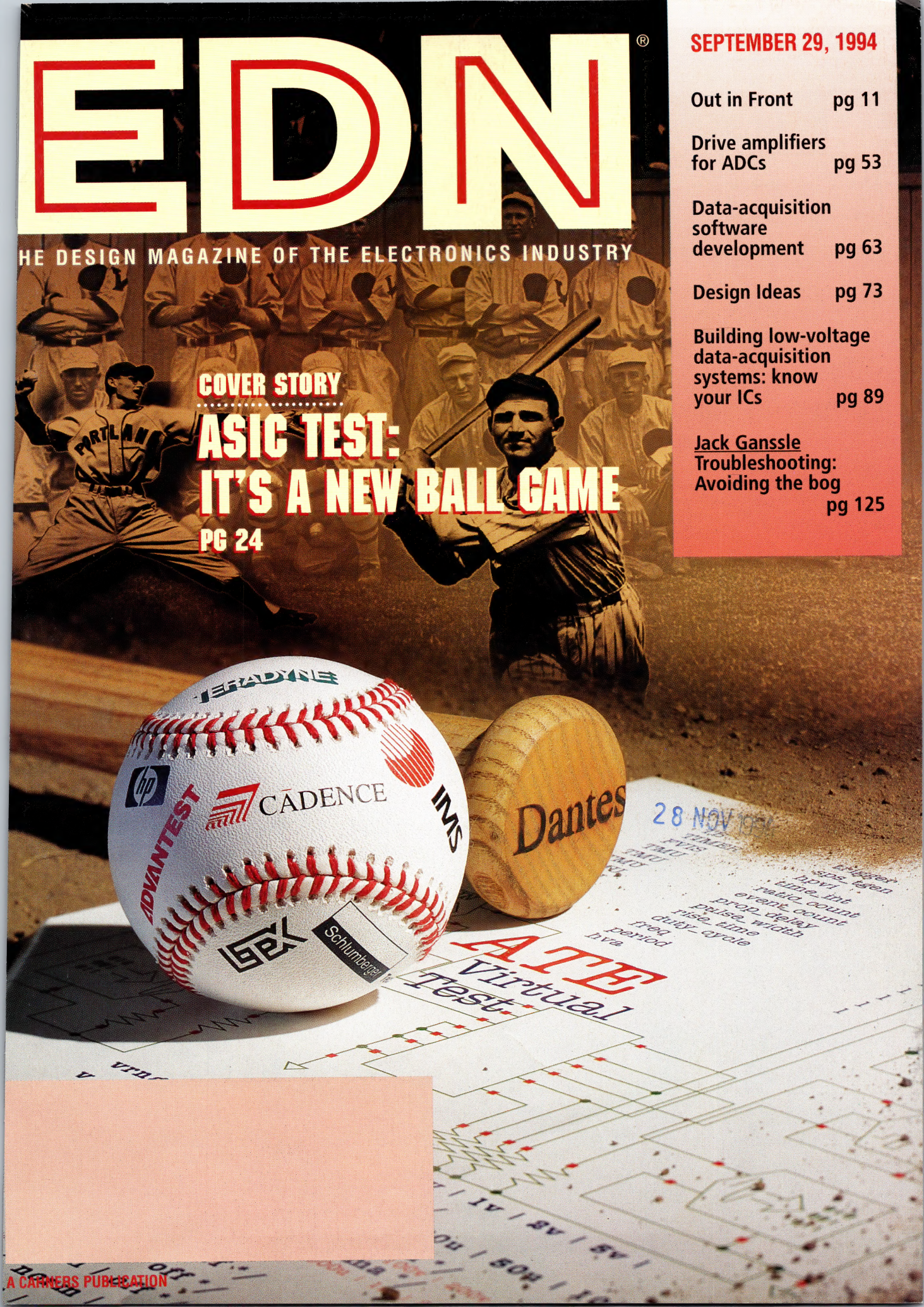
THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

SEPTEMBER 29, 1994

COVER STORY

ASIC TEST: IT'S A NEW BALL GAME

PG 24



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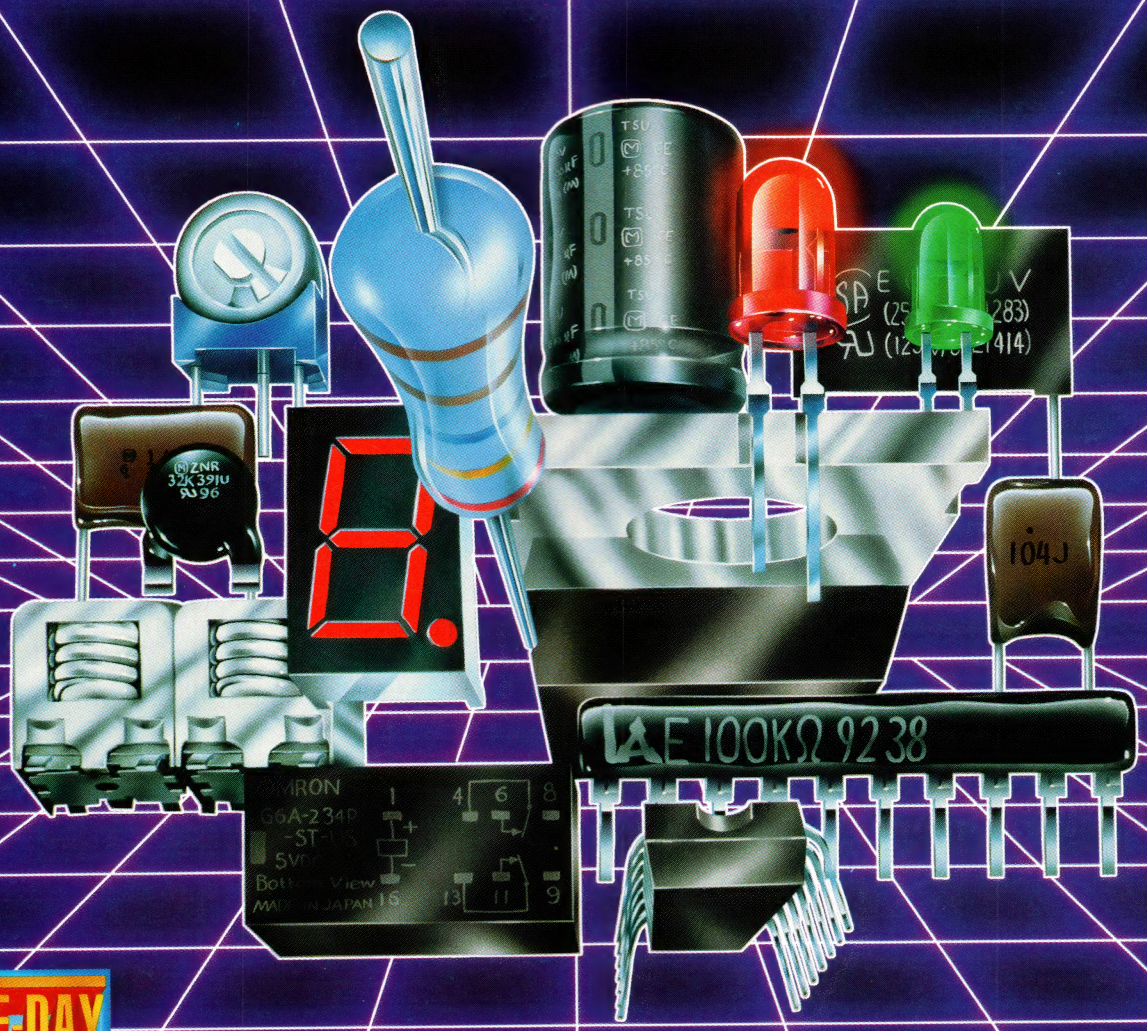

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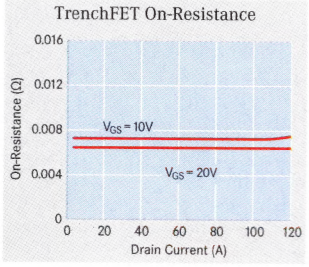

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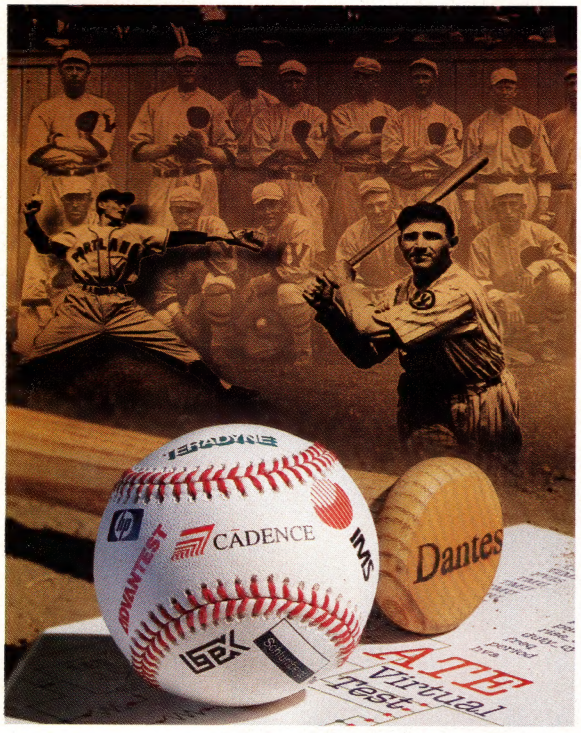

COVER STORY

ASIC test. Photo courtesy Cadence/IMS; historic images provided by the Oregon Historical Society. Design by Richard Anderson, Communications by Design; photography by Dahlstrom Photography Inc.

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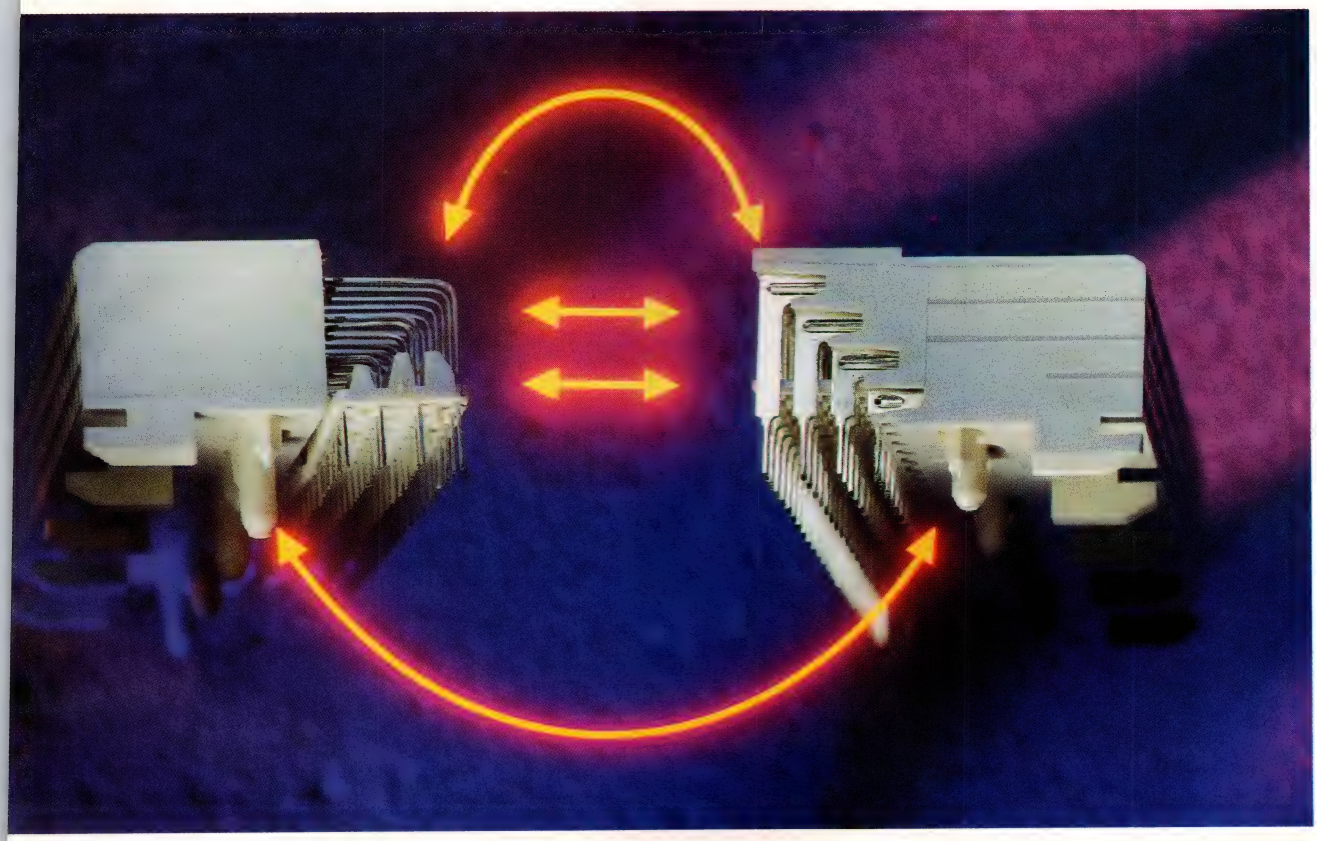

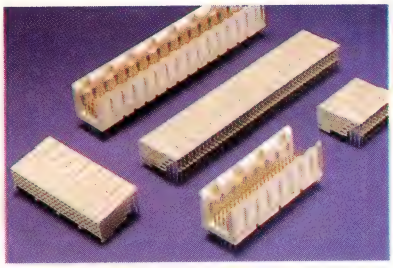

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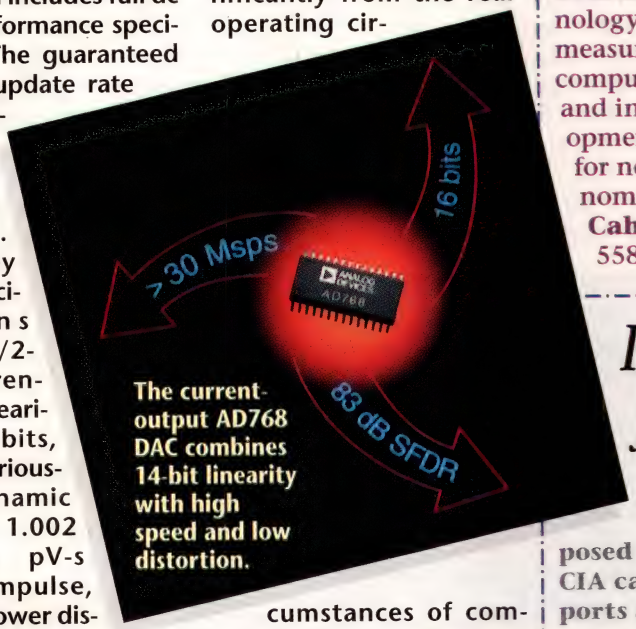
CIRCLE NO. 87

16-BIT DAC EXTENDS AC PERFORMANCE

The Analog Devices current-output AD768 combines the speed characteristics of 12-bit DACs with the precision of 16-bit devices and includes full dc and ac performance specifications. The guaranteed minimum update rate is 30M samples/sec; 40M samples/sec is typical. Other key typical specifications include 1/2-LSB differential nonlinearity at 14 bits, 83-dBc spurious-free dynamic range at 1.002 MHz, 35 pV-s glitch impulse, 465-mW power dissipation, and full-scale settling time of 25 nsec to 0.025%. Price is also a key feature of this DAC; at $19.95 (1000), it costs less than some of the company's 12-bit devices in the same speed range.

The manufacturer has also provided a glimpse into the DAC's performance for video-on-demand applications, such as an asymmetrical digital subscriber line (ADSL)—one of the standards ANSI is evaluating. Most DAC ac specifications are the result of tests with single-tone signals that differ significantly from the real operating circumstances of communications applications, which use spread-spectrum and frequency-division-multiplexed signals. The AD768's data sheet shows the following test result of a typical ADSL transmit chain: S/N ratio of 63.5 dB at 151 kHz and THD of –60 dBc at 160 kHz.



The current-output AD768 DAC combines 14-bit linearity with high speed and low distortion.

—by Anne Watson Swager

Analog Devices, Wilmington, MA, (617) 937-1428. **Circle No. 482**

VIEWLOGIC ANNOUNCES EDA BRIDGE. Viewlogic System and TEAM Corp have announced an EDA-bridge tool bar. The product presents Windows-style graphical icons for point-and-click control of frequently used commands and functions. According to the companies, the bridge makes Viewlogic's Pro Series CAE tools easier to learn and use.

TEAM Corp, Oakville, ON, Canada, (905) 842-1303. **Circle No. 483**

Viewlogic Systems Inc, Marlborough, MA, (508) 480-0881. **Circle No. 484**

Awards recognize outstanding engineers and products

EDN's annual Innovation and Innovator of the Year Competition honors outstanding engineering professionals who are committed to quality and creativity in electronics. The magazine presents innovation awards in the following eight major product/technology areas: ICs and semiconductors; μPs; test and measurement; electronic-design-automation tools; computers and peripherals; components, hardware, and interconnection technology; embedded development software; and power sources. Applications for nomination are *due by Nov 15*. Call *EDN* for a nomination package.—by Fran Granville

Cahners Publishing Co, Newton, MA, (617) 558-4681. **Circle No. 485**

Interface IC allows multiple functions on PCMCIA card

National Semiconductor's InfoMover PCM16C00 is the first communications interface circuit that implements the proposed PCMCIA multifunction standard for PCMCIA card designs. The InfoMover PCM16C00 supports any two I/O functions and memory that operate concurrently on a single PCMCIA card. The interface circuit seamlessly supports National's ST-NIC Ethernet controller device or any other LAN controller. The other function on the card could be a fax/modem chip set.

The challenge of implementing multifunctions on a PCMCIA card is that the host interface has only one interrupt-request (IREQ) line. Each function must use this line to get the attention of the μP in the main computer. Sharing the line can cause problems when more than one device driver attempts to use this line simultaneously.

In cooperation with the PCMCIA committee, National came up with an arbitration method for using the IREQ. The method employs priority or round-robin protocols, whichever the user prefers, informs the host system which function actually requires service, and arbitrates among them.

The multifunction circuit also offers power-management features that conserve battery life in portable or handheld computers. The PCM16C00 operates at 3.3 or 5V, and you can turn off or put into a sleep mode one or two functions on the card. In addition, the interface device supports hot-swapping so that you don't have to reboot the system when changing cards. The device comes in a 144-pin TQFP and costs $15 (1000).

—by John Gallant

National Semiconductor Corp, Santa Clara, CA, (800) 272-9959. Circle No. 486

ADC fits 14-bit, 10-MHz performance in small package

Datel's ADS-945 achieves its high-resolution, high-speed performance not in a power-hungry board-level design but in a 2×4-in. DIP with a package height of 0.29 in. At 4.5W, the 945's typical power consumption is less than 40% of the nearest small-package competitor. Key technical specifications include no missing codes to the 14-bit level over the industrial temperature range (–25 to +85°C), minimum S/N ratio of 78 dB, and maximum THD of –80 dB for dc to 1-MHz signals. The ADC, which includes a T/H amplifier, a reference, timing/control logic, and error-correction circuitry, costs $866 (100) for a commercial-temperature version. The industrial-temperature version costs $1079.

—by Anne Watson Swager

Datel Inc, Mansfield, MA, (508) 339-3000, ext 227.

Circle No. 487

Data-acquisition system streams 1M samples/sec to disk

BY COMBINING A PENTIUM PC containing a fast 1.7-Gbyte, SCSI hard drive with a 1M-sample/sec, 12-bit ADC board and some clever software, United Electronic Industries (UEI) has produced a system that can acquire nearly one-half hour of data nonstop at the ADC's top sampling rate. The hard drive is one of the "AV" types, which, unlike standard high-capacity drives, does not pause periodically for thermal recalibration of its read/write head. It's also removable; you can substitute a 3.02-Gbyte unit if you need to record even more data nonstop.

The $9750 system comes with a 17-in., high-resolution color monitor; selecting a 15-in. unit saves $250. You can also substitute other data-acquisition boards for the base system's Win-30D, or you can add a second board. The software runs under DOS. Part of its speed is attributable to its ability to pack four 12-bit conversion results into three 16-bit data transfers. If your acquired data set does not use too much of the room on the hard disk, the software rewrites the file onto the drive in a format that matches the requirements of the package you will use to postprocess the data. Moreover, UEI's software, which is available separately for $295 (source code, $695) lets you omit portions of the initial record from the final data file.

—by Dan Strassberg

United Electronic Industries, Watertown, MA, (617) 924-1155.

Circle No. 488

AT&T division to leave semiconductor market. AT&T Global Information Solutions (formerly NCR Corp) plans to leave the semiconductor market and to seek a buyer for its NCR Microelectronic Products Division. The company says the decision will free AT&T Global's resources, such as management time and R&D funds, to apply to information technology for the company's customers. The move does not affect AT&T's Microelectronics Division. **AT&T Global Information Solutions**, Fort Collins, CO, (303) 226-9527. **Circle No. 489**

PCMCIA card connects PC to MIL-STD-1553 bus

With a new PCMCIA card from ILC Data Device Corp (DDC), you can bring the power and convenience of portable computing to the MIL-STD-1553 data bus. The BU-65550 card provides an intelligent interface between a Type II PCMCIA slot and the dual-redundant 1553 bus, making the card useful for testing and system-integration tasks.

The card incorporates DDC's BU-61586 Advanced Communications Engine (ACE). The ACE includes dual transceivers and encoder/decoders, complete 1553 protocol, 12k words of shared RAM, and memory-management logic for the bus-controller, remote-terminal, and bus-monitor modes. Each card costs $3995.—by Gary Legg

ILC Data Device Corp**, Bohemia, NY, (516) 567-5600, ext 7381.* ***Circle No. 490

DILBERT® by Scott Adams

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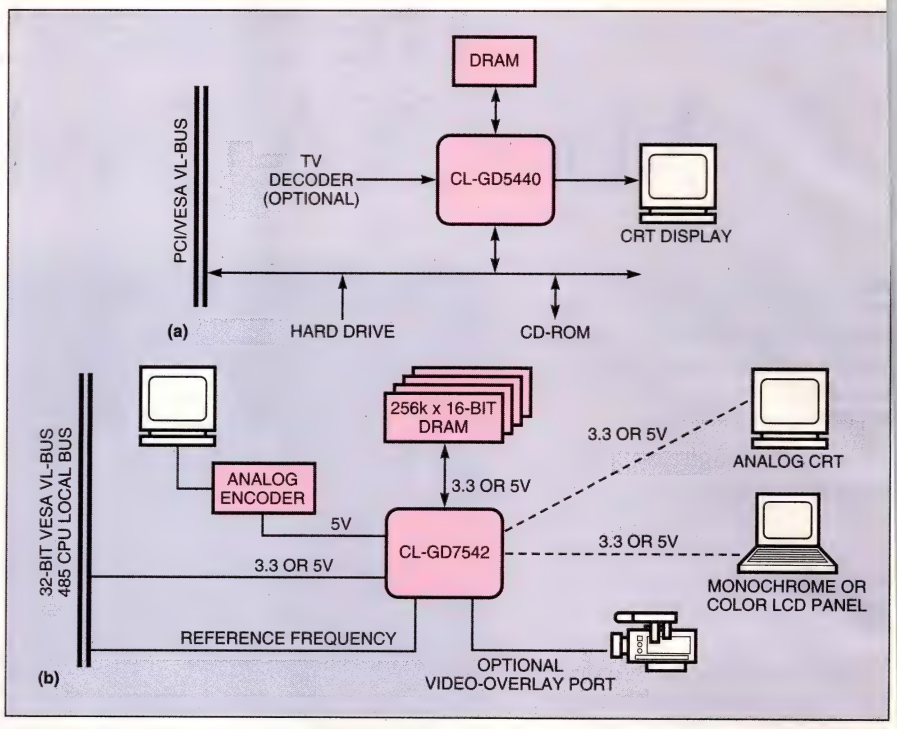
Chips lower cost of video playback

New ICs from Cirrus Logic allow low-cost implementations of video playback on both desktop and portable computers. For desktop designs, the CL-GD5440 provides video control and acceleration, and an optional CL-PX4072 multistandard TV decoder accepts NTSC, PAL, or SECAM inputs. For portable systems, the CL-GD7542 provides video control and acceleration with an optional video-overlay port. The cost to implement a video subsystem with the chips, excluding memory and depending on options, ranges from about $30 to $70 in OEM quantities. The ICs work on either the PCI or the VL bus.

Video subsystems designed with the new chips and 256k×16-bit DRAMs can display full-screen, full-motion (30-frame/sec) video. The two video-controller chips provide horizontal and vertical interpolation between incoming video pixels to scale a video image to screen size or smaller. The CL-GD5440 for desktops provides one- to four-times scaling; the CL-GD7542 for portables has two-times scaling. The number of available colors in desktop implementations ranges from 16 for 1280×1024-pixel displays to 64,000 for 800×600-pixel displays. For portable implementations, the color range is from 16 million for 640×480-pixel displays to 256 for larger displays. The CL-GD7542 for portables supports the new 800×600-pixel SVGA format and other formats. —by Gary Legg

Cirrus Logic, Fremont, CA, (510) 623-8300. **Circle No. 491**



New ICs from Cirrus Logic implement video playback on desktop systems (a) and on portables (b).

Clamped amplifiers jump in accuracy and add a surprise

The AD8036 and AD8037 from Analog Devices offer high linearity and clamp accuracy—an order of magnitude improvement over existing clamped amplifiers. In addition, an engineer at the company found another benefit of the devices: You can easily configure them as full-wave rectifiers, in one case by connecting the noninverting input to the high or low clamp inputs. You can even put a modulating signal into the high and low clamp inputs, which each have a bandwidth of at least 100 MHz.

A proprietary design that implements the clamping at the amplifier input as opposed to the output provides the very high clamp accuracy that makes additional applications possible. Maximum and typical output deviations from the clamp voltage setting are ±25 and ±15 mV, respectively. The design also minimizes signal distortion near the clamp voltages and allows for a maximum useful amplifier range. You can set the clamp voltage, for example, to any value in the ±3.9V output range.

In the unclamped region, these 250- and 275-MHz amplifiers also have very low distortion; they are cousins of the recently introduced wide-bandwidth, ultra-low-distortion 320-MHz AD9631 and 250-MHz AD9632, which boast a spurious-free dynamic range of –72 dBc typical at 20 MHz. The AD8036 is unity-gain stable, and the AD8037 is stable for gains of +2; you must use both in noninverting configurations. Settling time to 0.01% accuracy is 16 nsec. All of these low-distortion amplifiers cost $4.12 (1000). One main application for all these devices is driving high-speed, high-resolution ADCs (see "Drive amplifiers for ADCs" in this issue). —by Anne Watson Swager

Analog Devices Inc, Wilmington, MA, (617) 937-1428. **Circle No. 492**

Current-feedback amps increase in accuracy

"Precision" and "accuracy" are two words not usually associated with current-mode feedback amplifiers. These amplifiers' claim to fame is high bandwidth without the familiar gain-bandwidth roll-off of voltage-feedback amplifiers. However, Elantec Corp is combining precision and current feedback in the form of the EL2165C and the EL2175C. These amplifiers provide designers of high-speed-instrumentation, video, imaging, and communications systems with much better dc characteristics than are available in conventional current-mode feedback amplifiers. With –3-dB bandwidth for gains of +2 at 30 and 120 MHz, input offset voltage is

(Continued on pg 16)

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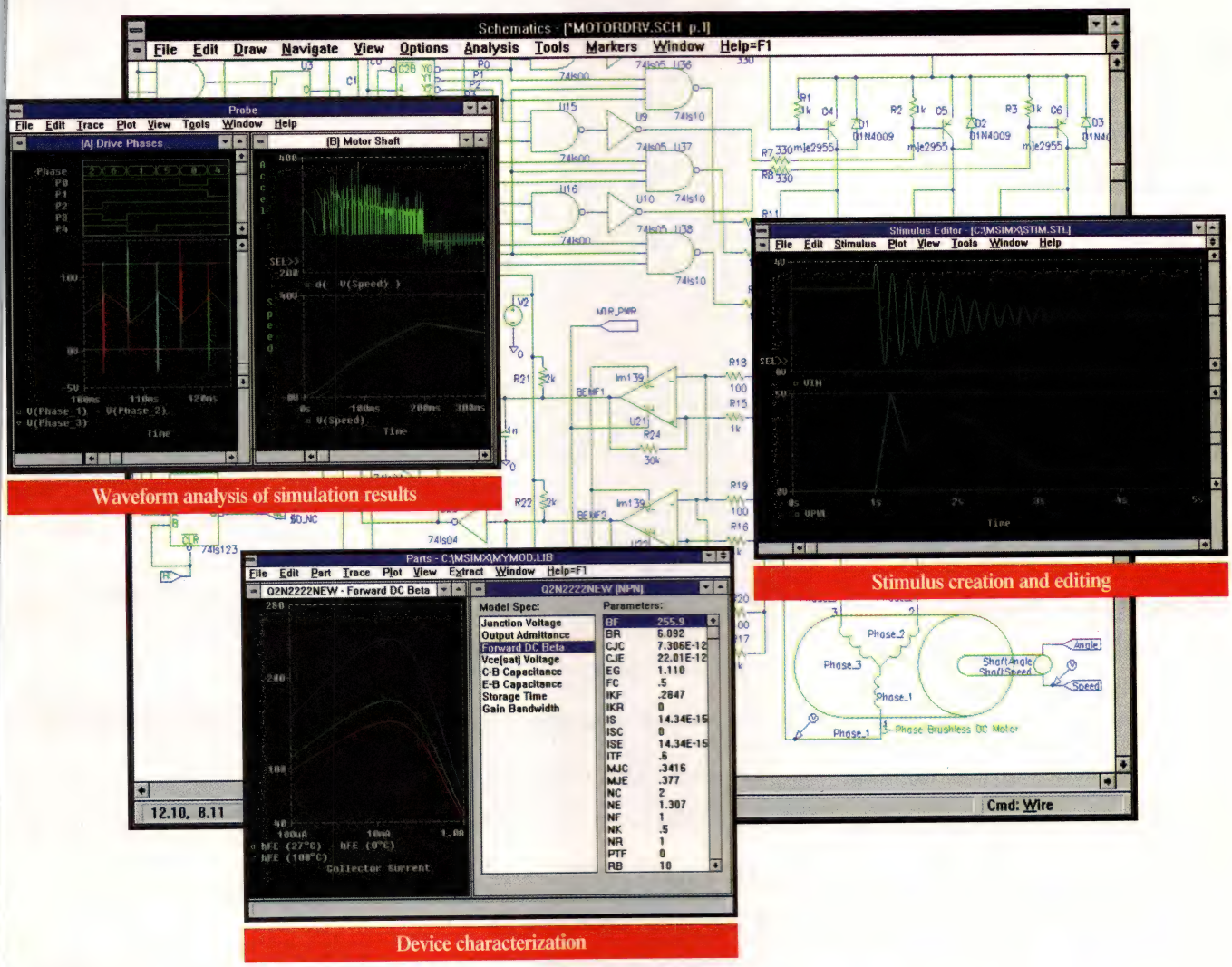

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500 μV, and negative input-bias current is 500 nA. Respective peak-output currents are 50 and 80 mA. The 2165C consumes 4 mA, and the 2175V consumes 8.5 mA. The 2165C settles to 0.1 and 0.01% in 110 and 185 nsec. Both operate on supplies ranging from ±3 to ±16V and provide input/output compliance to within 2V of the supplies. Respective settling times to 0.1 and 0.01% are 110 and 185 nsec for the 2165C and 55 and 85 nsec for the 2175C. The devices come in 8-pin DIPs and SOICs, and prices start at $2.67 (1000). Samples will be available this month. (All listed specifications are for typical performance.)

—by Anne Watson Swager

Elantec Corp, Milpitas, CA, (408) 945-1323. **Circle No. 493**

Wider tape boosts minicartridge capacity

New QIC-Wide products from Conner and Sony enable a QIC tape minicartridge to store 420 Mbytes of compressed data, conveniently keeping pace with storage capacities of the disk drives in many new high-end PCs. Sony's QIC-Wide media is responsible for the high capacity, providing a 68% increase over typical 250-Mbyte QIC-80 minicartridges. Conner's 11250M tape drive, which uses the new media, is also compatible with standard QIC media.

QIC-Wide tape is 0.315 in. wide, compared with 0.25 in. for QIC tape. Because the extra width provides additional strength, Sony can make the tape thinner and thus pack more of it into a minicartridge—400 ft vs the usual 307 ft. A redesigned Conner tape-drive head accommodates the wider media, and modified tape-drive firmware ensures QIC and QIC-Wide compatibility. An internal-mount version of the new Conner drive sells for $114 (OEM); an external, parallel-port model costs $244. A Sony minicartridge two-pack will sell for under $50. —by Gary Legg

Conner Tape Products Group, Costa Mesa, CA, (714) 641-1230. **Circle No. 494**

IC ATE systems economize on pin electronics

Today's digital ICs often have pin counts in the hundreds but operate at maximum speed only on a fraction of their pins. Integrated Measurement Systems (IMS) has found a way to save sizable sums for purchasers of testers for these devices. Instead of following the industry custom of providing the same performance on all pins, for its ATS Blazer! system, IMS has designed a 100-MHz pin-electronics card that is mechanically and electrically interchangeable with the system's 200-MHz card. The 200-MHz card uses a mixture of silicon and GaAs ICs to achieve its performance; the 100-MHz card uses silicon devices exclusively and is, therefore, substantially less expensive. A 320-pin system one-third of whose pins operate at 200 MHz costs less than half of the $1.6-million cost of competitive systems that have the same number of pins, all capable of running at 200 MHz.

At the same time (that is, at next week's International Test Conference in Washington, DC), IMS parent, Cadence Design Systems Inc, in conjunction with the Industrial/Consumer Division of automatic-test-equipment vendor Teradyne Inc, will announce a pair of enhanced packages for development of programs for testing mixed-signal ICs. Version 2.0 of Cadence's Dantes virtual-test software, integrated with Teradyne's Image ExChange test-event simulator, enables test engineers to verify device-test programs without waiting for first silicon and without taking time on a tester. (See this issue's cover story on pg 24.)

—by Dan Strassberg

Cadence Design Systems, Beaverton, OR, (503) 626-7117. **Circle No. 495**

Integrated Measurement Systems Inc, Beaverton, OR, (503) 626-7117. **Circle No. 496**

Teradyne Inc, Boston, MA, (617) 422-2567. **Circle No. 497**

MOS-controlled thyristors get some backup

Harris Semiconductor is extending support for its MOS-controlled thyristor (MCT) with the HIP2030 gate driver, which also simplifies designing with high-power insulated-gate bipolar-transistor (IGBT) modules. To drive an MCT previously required one dual FET driver, two FETs, two diodes, two capacitors, and 11 resistors. Designed by Harris and available since 1992, MCTs are power-switching devices that provide a two-times current-rating increase over IGBTs along with a lower forward voltage drop in the same die size. MCTs are useful in power-switching applications at rates up to around 100 kHz whenever high current and low conduction loss are prime requirements.

MCTs may seem more complicated to use because they require a dual-polarity control signal, but many IGBT manufacturers now recommend using similar control signals for IGBTs because of their large gate capacitances. By switching the polarity of its output and adjusting two resistors to obtain the desired voltage levels, the HIP2030 can drive IGBT modules. The HIP2030 ($5.50 (1000)) can drive 60 nF of MOS capacitance with 30V p-p in less than 200 nsec and 15 to 20 nF in less than 100 nsec. The IC also includes a charge pump so that it can operate from a single low-voltage supply as well as from the single or dual high-voltage supplies that provide the MCT gate-drive voltages. A latch/reset circuit can inhibit drive to the MCT gate in the event of excessive load current or overheating.

—by Anne Watson Swager

Harris Semiconductor, Melbourne, FL, (800) 442-7747, ext 7267. **Circle No. 498**

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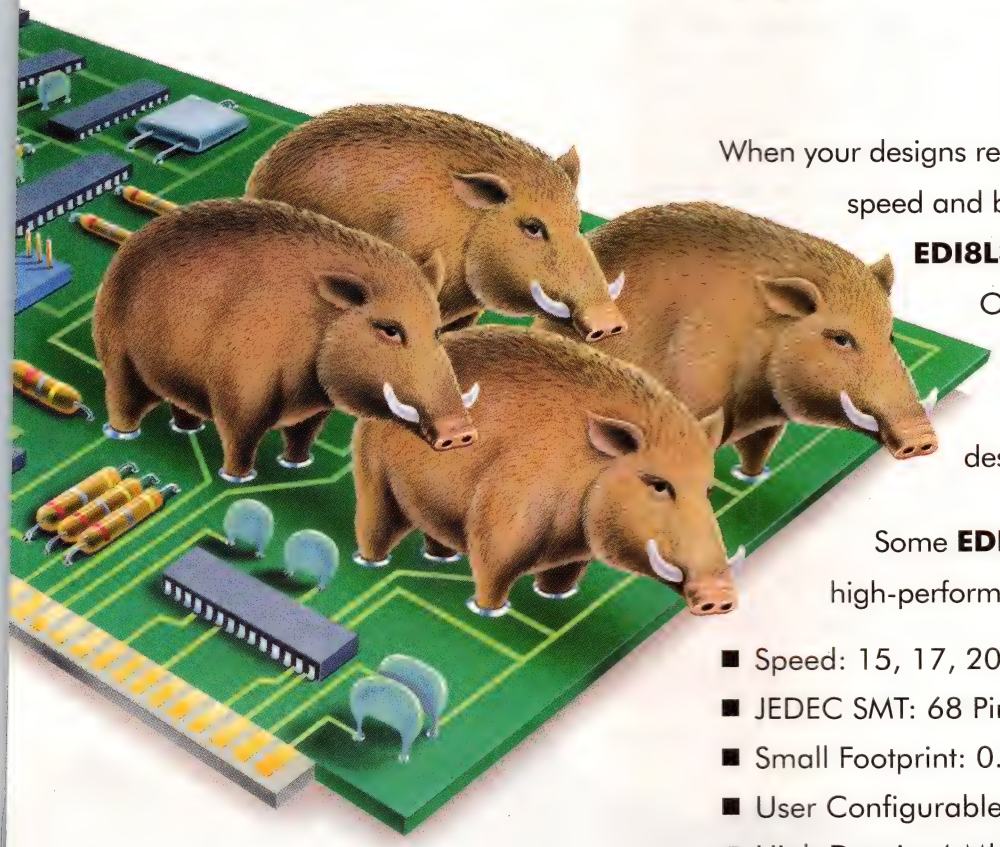

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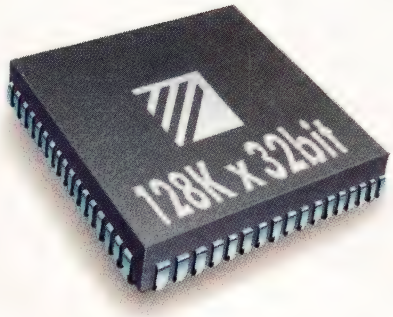

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VXI: One big, happy family at last?

"We must all hang together, or assuredly, we shall all hang separately," said Benjamin Franklin more than two centuries ago. In a similar spirit, the VXI Plug-and-Play Systems Alliance welcomed its newest members at a meeting in Austin, TX, in mid-July. Among the seven companies joining the alliance is the group's largest and, arguably, most influential member—Hewlett-Packard. Market researchers claim that HP has captured 38% of the revenues for VXI instrumentation, the largest share of any vendor. HP owes its lead to many factors, not the least of which is its broad line of VXI hardware.

What users want is assurance that, by adopting VXI, they are placing their bets on a leading-edge technology that has staying power.

Notwithstanding a strong VXI software entry, the VEE graphical programming system (available both for Unix workstations and Windows PCs), HP's share of VXI software sales is not the largest. Software market-share honors go to National Instruments. NI's VXI products include LabWindows for MS-DOS, LabWindows/CVI for Windows PCs and Sun Workstations, and the LabView graphical programming system for the Macintosh, Windows PCs, and Unix workstations.

About a year ago, several companies formed the VXI Plug-and-Play Alliance. Alliance founders realized that for VXI to make good on its early promise, VXI systems integrators had to be able to put together systems using components from any VXI vendor and be assured that the hardware and software would play together. If problems developed, users would not tolerate a group of vendors who pointed fingers at each other. By spring of this year, the Alliance membership had grown to nearly 20 VXI vendors.

Whether or not the perception was correct, the formation of the Alliance created an impression that the VXI community was polarizing into two camps. One camp, comprising Alliance members, was headed by National Instruments with its lead in VXI software. The other camp, headed by HP, offered a broad line of high-quality hardware and credible software. Within either camp, the level of compatibility was high, although not as high as necessary. Between camps, even if outright animosity didn't exist, the level of compatibility was unacceptable.

The problem with this state of affairs was that the VXI community could ill afford to rend itself asunder. Despite some attractive competing technologies, a united VXI community can succeed. But VXI would mortally wound itself if vendors tried to gain the upper hand by labeling certain VXI products inferior because of incompatibilities with their own products. Such an approach would not only dissipate the energies of VXI vendors; it would send precisely the wrong message to potential users. What users want is assurance that by adopting VXI, they are placing their bets on a leading-edge technology that has staying power. Users want to know that their investment will be preserved by the continued availability of products and support services from a wide variety of vendors. To achieve a lower cost of ownership over the life of their systems, these users will pay a premium for initial purchases.

Now that the VXI Plug-and-Play Alliance has set the stage for cooperation among all VXI vendors, the vendors must deliver on that promise. HP, the company with the most resources, faces the biggest challenge: producing C-language versions of several hundred instrument drivers. The new drivers, which will be just as compatible with VEE as HP's current drivers, will also be compatible with LabWindows/CVI. Indeed, HP may get help in this effort from National Instruments, because NI already has LabWindows/CVI drivers for many HP VXI modules. The result will be that users of HP hardware will be able to use NI software—if they choose to, and vice-versa.

What transpired in mid-July in Austin was surely a watershed event for VXI. But its significance for the rest of the industry is even greater. VXI began in 1987 with a spirit of cooperation among competitors who realized that their own interests would be served if they placed customers' interests first. Just when it looked as if that spirit of cooperation was unraveling, the VXI Plug-and-Play Alliance resurrected it with a vengeance.

How much time must pass before other electronics market segments realize that this type of customer-focused cooperation can also pay big dividends to vendors?

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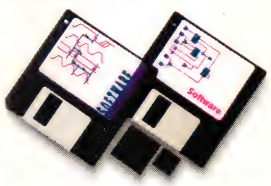

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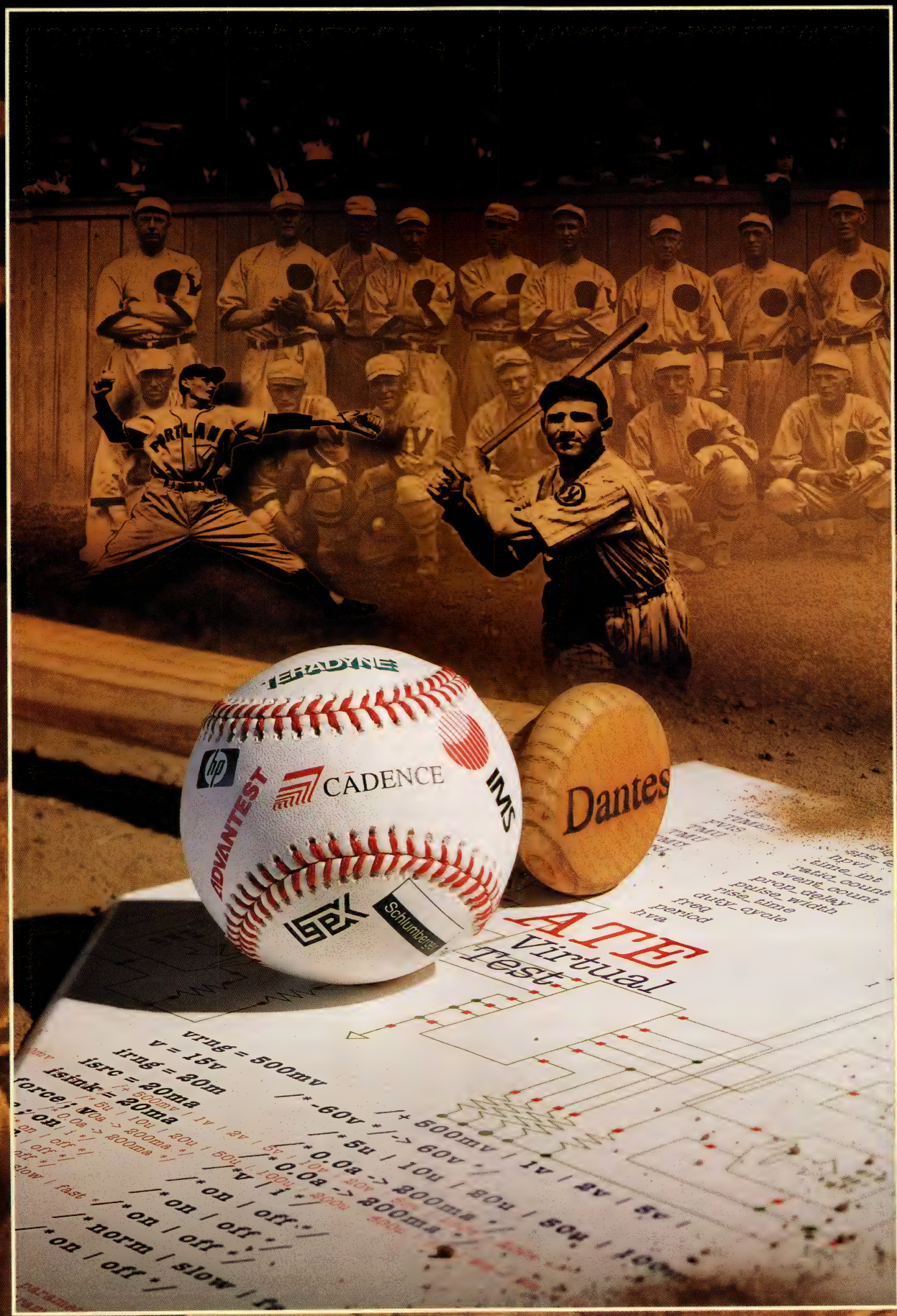
ASIC TEST

IT'S A NEW BALL GAME

DAN STRASSBERG, SENIOR TECHNICAL EDITOR

Testing ASICs means more than just designing for test. Although today's sophisticated DFT tools are a big step forward from earlier ones, intelligently tackling test requires a partnership between design and test—and designers' full appreciation of what test is all about.

Even if you think you know all you need to about ASIC test, don't turn the page quite yet. Sure, you know that, thanks to structured design methods, you can create chips of incredible complexity in less time than it took to develop devices only one-tenth as complex just a few years ago. And you probably also know that, in some cases, structured design-for-test (DFT) techniques can reduce creating test patterns to a pushbutton operation that takes less than a day on a workstation. A few years ago, pattern generation, performed manually, was a tedious, error-prone ritual that could consume months.



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That's the good news about ASIC test. But there is a dirty little secret too—a part that too many design engineers have tried to pretend doesn't exist: Making sure before you have silicon that the devices will be testable when silicon finally arrives requires much more than turning an automatic-test-pattern-generation (ATPG) package loose on the design. Test-development can still take months and, in the case of mixed-signal ICs, sometimes stretches to over a year. But there's more good news: Suppliers of electronic-design-automation (EDA) tools and automatic test equipment (ATE) are introducing a host of products to automate dozens of tasks that are essential for developing adequate tests. Designers previously performed these tasks by hand.

Classical gate-level stuck-at fault simulation for circuits not designed with the use of DFT methodologies is inherently computation-intensive; the operation can take weeks, even on a powerful workstation. Specialized hardware accelerators, like these Paradigm XP units from Zycad Corp, can cut fault simulation times by as much as two orders of magnitude.

These tools fit into a category called "virtual-test" (VT) tools. Cadence Design Systems was among the first to use the term in connection with IC test but has not applied for a trademark and has no plans to apply for one. Indeed, the company would be happy if other vendors began using the phrase. Marv Wolfson, vice president of Cadence's test-software business, thinks that such acceptance would enhance the concept's credibility. Nevertheless, because there is no universally agreed-upon scheme for categorizing EDA tools, Wolfson is concerned that other companies could confuse users by attempting to alter Cadence's meaning.

That meaning is specific: VT tools allow test engineers to create, optimize, simulate, and debug test fixtures and device-test programs that can run on ATE systems. VT tools' main goal is to shorten product-development cycles through more efficient use of test-engineering resources. The tools, which begin by taking input from the device's design database, allow users to complete most test development *before* silicon becomes available *without* tying up scarce and expensive ATE.

An added benefit is the tools' ability to reveal device-design problems that affect testability. Through VT, users can demonstrate that devices are testable *before* transmitting the designs to a foundry. Designers who learn about test problems soon enough can modify their designs to eliminate the need for costly work-arounds or even costlier mask redesigns. VT recognizes that the roles of design and test engineers are complementary and that test engineers are designers, albeit not of products—but of the fixtures, test programs, and procedures that make possible economical production of high-quality products.

Don't be confused by the seeming similarity between VT tools and a more familiar type of EDA tool, the design-rule checker. To be sure, both types of packages help to ensure testability, but design-rule checks occur earlier in the design cycle—before the insertion of the chip features that provide testability. Design-rule checking aims to verify that automatic test-structure insertion packages can, in fact, add features that

THE TORTUOUS PATH TO IC QUALITY

"Tortuous:" the dictionary defines it as "winding, twisted...complex." Electronic-design-automation (EDA) tool vendors have spent countless person-years developing tools that make the path to IC quality less tortuous. Although these efforts have achieved considerable success, the path is still not straight or smooth. Part of the reason is that most of the efforts focus on the first two categories in the test-development-automation tool list on the next page: design-for-testability (DFT) and pattern-development tools.

DFT tools in particular are used early in the design process. In most companies, the users are design engineers—the traditional audience for EDA products. Users of pattern-development tools are more varied. In some companies, test-pattern development is a design function. In other companies, the job falls to test. In a few cases, netlist files go off to a foundry, and the foundry generates the test patterns.

Test engineers working in IC-fab facilities are most likely to use virtual-test (VT) tools. Although design verification and manufacturing test have different objectives, putting responsibility for VT too far from design can result in test programs that fail to find critical device defects. Despite the capabilities of the design-rule-checking packages used earlier in the design process, projects that wait too long to use VT tools miss a golden opportunity to correct design flaws while they can still be corrected at moderate cost. Undoubtedly, the probability that both the first silicon and the first iteration of the test program will work as desired improves dramatically as cooperation between design and test goes up.

provide high fault coverage. As part of creating test packages, VT tools can complement design-rule checking by proving that rule checking has achieved its goals.

The most appropriate term for the universe of tools involved in ASIC test is "test-development automation" (TDA) tools. (Some vendors use the term "test-automation," but the tools, most of which are software, don't automate testing; ATE does that. The tools automate various aspects of test development.) The **box**, "The tortuous path to IC quality," and the **table**, "Test-development-automation tools," indicate the types of tools and their significance in test development. The listings should shed light on the roles of classes of tools. In the manufacturers' **box**, you'll find names of EDA suppliers that offer TDA tools as well as names of vendors of semiconductor ATE systems.

According to Ben Bennetts, senior test consultant at Synopsys, achieving a testable design for a digital IC involves the following five primary steps, which Bennetts attributes to Robert Aitken of Hewlett-Packard:

- Design-rule checking to make sure that the design conforms to the rules for the chosen DFT methodology or methodologies—full or partial scan, built-in self test (BIST), boundary scan, or IDDQ (a technique for CMOS ICs that finds faults by measuring a chip's quiescent supply current, I_{DDQ}). The rule-check preconditions the circuit for the insertion of test structures that implement the chosen methodologies.
- Test-structure insertion—for example, conversion of D flip-flops into scannable latches. Test-structure insertion is often called "test synthesis"—another somewhat misleading term. Test synthesis doesn't synthesize tests; it synthesizes silicon structures that make it convenient to design tests.
- Global reoptimization to assure that the design that now includes test structures meets the original constraints on such factors as timing, area, output-drive capability, and power dissipation.
- Test-pattern generation, or the generation of test patterns that, when applied to the circuit, make faults observable.
- Fault simulation and fault-coverage grading of test-vector sets. Fault-coverage grading, is commonly referred to as "fault grading," doesn't grade faults; it grades vector sets' ability to detect faults.

TEST-DEVELOPMENT-AUTOMATION TOOLS

Design-for-testability (DFT) tools (test-synthesis tools)

- Testability-analysis tools
  - Design-rule checkers
    - PLD testability-analysis tools
  - Stuck-at fault-simulation and vector-grading tools
  - Hardware accelerators for fault simulation
  - Delay-fault simulators
- Test-structure insertion tools
  - Boundary-scan-structure insertion tools
  - Internal-scan-structure insertion tools
  - Partial-scan tools
  - BIST-structure insertion tools
    - Regular-structure BIST insertion
    - Random-logic BIST insertion
  - Tools for inserting IDDQ-initialization structures

Pattern-development tools

- ATPG
  - Full-scan ATPG
  - Partial-scan ATPG
  - Sequential ATPG (Ed note: such as it is)
  - Boundary-scan vector generators
  - IDDQ vector-generation tools
    - Tools for predicting IDDQ and setting test limits
- Vector-compaction tools

Virtual-test tools

- EDA-related
  (Tools that support ATE from more than one supplier)
  - Test-rule-checking tools
  - Test-schematic-capture tools
  - Test-documentation tools
  - Tools for automating test-fixture design and layout
  - Test-fixture-simulation tools
  - Tester-resource-simulation tools
  - Signal-analysis tools
  - Format-conversion tools (also see tester-specific VT tools)
- Tester-specific
  (Tools specific to particular ATE systems or systems from one supplier)
  - Format-conversion tools (also see EDA-related VT tools)
  - ATE system software
    - Test-sequencing tools
    - Test-optimization tools
    - Test-debugging tools
  - Test emulators (also called test-event simulators)
  - Tools for off-line test-program development

Although modern test-pattern generators include fault simulators, free-standing fault simulators can still be useful. Such simulators start with functional vectors (developed for design verification). These vectors provide structural-defect coverage without additional effort. Functional vectors usually provide 40 to 50% fault coverage and often catch timing-related faults. Whereas fault coverage of 40 to 50% is usually not adequate for production test, it can be a good starting point. Moreover, timing-fault coverage is something that scan-test vectors don't normally provide.

Even though these five steps go a long way toward assuring testability with a specified degree of fault coverage, they do not, in general, complete the job of producing a testable design. That job involves steps such as design and debugging of test fixtures and test programs. Although the test vectors that ATPG tools create are the most important elements of a test program, they aren't the program. Moreover, until you debug the test fixture and test program, design problems that affect testability may remain hidden. This is especially true when devices are complex or have appreciable analog or mixed-signal content or when the specifications push process limits or tax test-equipment capabilities.

An objective of virtual-test tools is to minimize the likelihood that the test fixture, test program, or ATE idiosyncrasies can interfere with valid and adequate testing. To be useful for this purpose, the tools must not add appreciable delays to the design cycle. Design engineers and program managers cannot tolerate a process that delays the transmission of a design to a

ASIC TEST

foundry by more than a few days.

However, the need to rush products to market is no greater than the need to turn over every stone when looking for device faults. Semiconductor test and process engineers often use the following equation to determine how high a test process' fault coverage must be. Although some of the assumptions underlying the equation are open to question (uniform density of defects across the wafer, for example), nobody has come up with a technique for calculating required fault coverage that is easier to apply or in which reliability experts have more faith.

$$DL=1-(Y^{1-FC}),$$

where DL=defect level (the portion of devices that pass the test but are, in fact, defective), Y=yield (the portion of all devices tested that are good), and FC=fault coverage (the fraction of all possible faults that the test can finding).

If DL=1000 ppm=0.1%=10^{-3} and FC=0.9,

$$10^{-3}=1-(Y^{0.1})$$

$$Y=0.991.$$

Thus, if the fault coverage is 90% and you can't tolerate more than 0.1% bad devices' getting through your test process, you must be confident that the manufacturing process (before testing)

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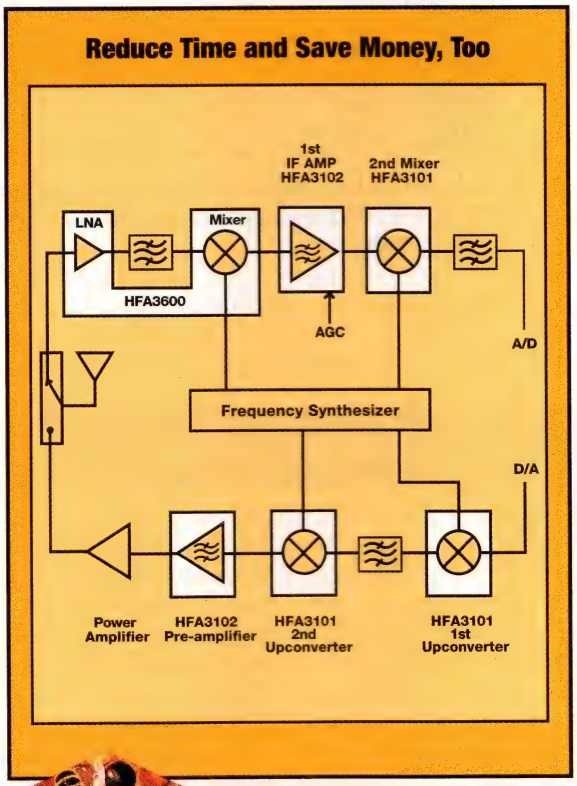

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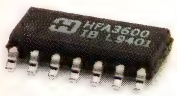

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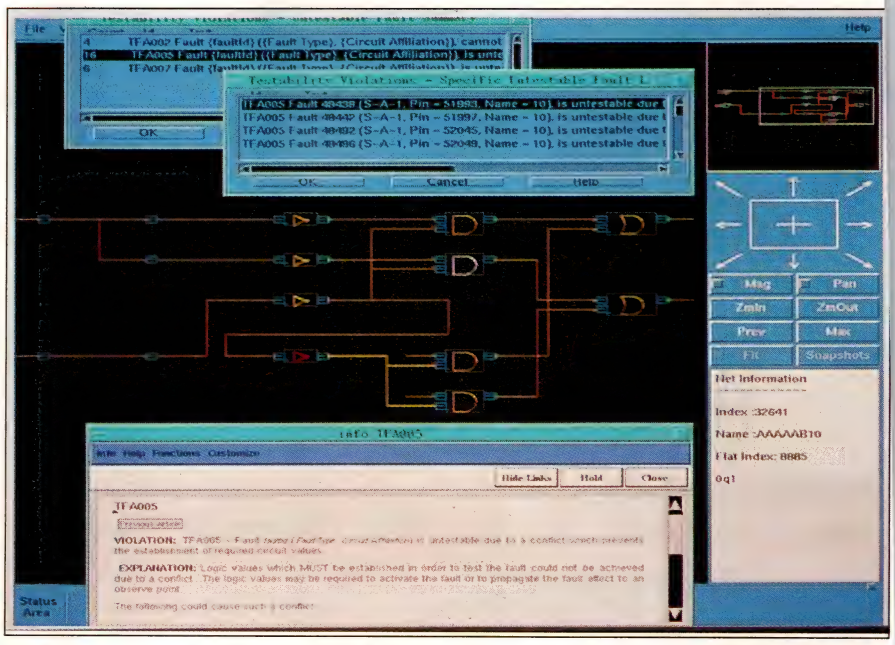
If Y=0.8 and FC=0.9, DL=0.022.

In other words, if the fault coverage is 90%, and 80% of the devices you send to test are good, 2.2% of the devices that test tells you are good, are, in fact, defective.

In today's market, few applications can tolerate defect levels as high as 1000 ppm, let alone 2.2%. Most applications, even commercial ones, require defect levels no higher than 200 ppm. The message is clear: 90% fault coverage is rarely adequate. Adding to the problem of achieving adequate fault coverage is the assertion that devices that purportedly can be tested with 100% fault coverage using scan-test vectors actually achieve fault coverages no higher than the low 90% range when tested with functional vectors. If this assertion is correct and if the faults detected in functional testing are not delay faults—which scan does not claim to catch—the allegation that scan-test vectors provide less than 100% coverage raises doubts about the effectiveness of scan methodologies.



Packages such as TestBench from Altium perform design-rule checks. In this screen, the graphic display indicates a conflict that prevents a fault from being activated or propagated.

Because no single test method reveals every fault, if you need a low rate of test escapes (defective devices that escape detection in test), you need to use a combination of test methodolo-

LOOKING AHEAD

In IC test, as in so many other areas of electronics, a wonderful synergy is developing. That synergy—between structured design and test-development automation (TDA)—will make test development faster and easier and will make testing more effective. Alas, though, like nearly everything else the electronic-design-automation (EDA) industry touches, new, improved, TDA tools are unlikely—at least at first—to live up to vendor promises. (Users would have walked away long ago from most industries with the EDA industry's sorry record of overpromising. EDA users have little choice, however; they can't do their jobs without EDA tools. Fortunately, EDA vendors usually deliver promised tools to those who can wait long enough.)

The most important incentive to implement TDA is the continuing march toward greater IC complexity. That march is possible only because of the use of top-down design methodologies. From a test viewpoint, top-down design can remove the designer too far from the gate level. But, since you really have to think at the gate level (and maybe even at the transistor level) to achieve good fault coverage, you have to look to new technologies to make sure that complex devices are tested adequately. The new technologies are automatic test-structure insertion (test synthesis) and automatic test-pattern generation (ATPG).

Test synthesis and ATPG aren't panaceas, however. For example, many informed industry observers doubt that ATPG will ever become a reality for sequential circuits. And, except when used on designs for relatively simple devices of moderate performance, ATPG doesn't come close to doing the whole test-engineering job. Thus, virtual-test tools should become important components of test engineers' arsenals. Marketing those tools effectively poses a challenge to the EDA industry, however.

With the exception of a few companies, EDA companies do not have close ties to test engineers. (Summit Design—formerly TSSI—is probably the most notable exception. Cadence, thanks to its ownership of ATE vendor Integrated Measurement Systems—IMS—is another.) The challenge for EDA companies is to develop the ties with test engineers that they already enjoy with design engineers. Clearly, EDA vendors have been courting the test community; for several years, many EDA companies have been highly visible at the International Test Conference. (The 1994 edition of the conference will take place on Oct 3, 4, and 5 in Washington, DC.)

Nevertheless, any EDA vendor that seriously intends to do business with the test community must do more than appear at industry events. A word of advice to the vendors seems appropriate here: If you think design engineers are cynics, get to know a few test engineers! The way to test engineers' hearts definitely is *not* through excessively optimistic product-performance and delivery claims.

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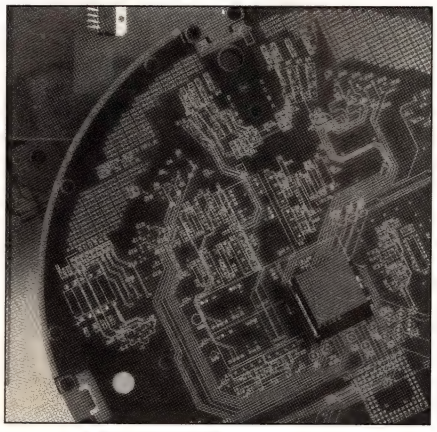
gies: full scan on portions of the chip that are amenable to full scan, partial scan elsewhere, boundary scan on the I/O lines, BIST on structures such as RAM, IDDQ to detect faults that elude the other methodologies, and possibly some delay-fault testing. Although such a mixed approach may sound too complex to be practical, industry experts are nearly unanimous on its validity. Moreover, with the right suite of test-development tools, you can achieve high fault coverage more easily by mixing methodologies than by doggedly applying a single, sometimes inappropriate, approach.

IDDQ is a promising technique. Thanks in part to a well-documented study that has become an industry classic (**Ref 1**), the approach is starting to see broad application. IDDQ has several advantages: It imposes minimal constraints on chip designers. Although it may be advisable to add structures to the silicon that initialize the chip for IDDQ tests, such structures aren't mandatory. Creation of IDDQ vectors requires minimal knowledge of a chip's operation. You need no more than a few hundred IDDQ vectors to provide high fault coverage—even for chips with half a million gates. And, although definitive studies are still lacking, several people familiar with the technology expect to see a high correlation between I_{DDQ} and delay faults.

That's the good news about IDDQ testing. The bad news is that, today, the tests are so time-consuming that few foundries apply more than a small fraction of the IDDQ vectors needed to achieve high fault coverage. (The number of vectors applied usually is under 20. Such limited IDDQ tests act as an adjunct to functional and scan tests.) IDDQ tests are slow because you must measure tiny currents—microamps at most—and, on ATE systems, only the slow pin-measurement units can perform the task. Help is on the way, though. An industry group called QTAG (the name was adapted from JTAG, the Joint Test-Action Group that ultimately became the IEEE-1149 Boundary-Scan Committee) will shortly announce a design for a bipolar current-to-voltage-converter IC housed in an eight-pin SOIC package that test engineers can mount on device-under-test (DUT) boards. The IC significantly speeds IDDQ testing by supplying a voltage proportional to I_{DDQ} that ATE systems' high-speed hardware can measure.

A second problem with IDDQ is that setting test limits often involves a trial-and-error process, which, in turn, requires actual devices. However, software to predict the levels of I_{DDQ} in good devices should arrive soon, allowing designers to set test limits accurately before the arrival of first silicon.



With high-performance and mixed-signal ICs, designing for test involves more than developing a set of test vectors. A critical component is the board that connects the device under test (DUT) to the automatic test system. Teradyne's A500 series test systems for analog VLSI ICs use boards like these.

Still only a few VT products

Whereas nearly half of the *types* of TDA tools fall into the VT category, less than half of the available TDA *products* are VT tools. VT tools complement—but do not replace—the more classical DFT and ATPG tools. To be sure, designs of certain types—mixed signal, for example—need VT more than do other types of designs. The most ambitious EDA-related VT tool is probably Cadence's Dantes (an acronym derived from design and test engineering system) for analog and mixed-signal designs.

Version 2.0 of the two-year-old tool will debut at the 1994 International Test Conference in October. Among its capabilities is test-rule checking to make sure that proposed tests do not ask the test equipment to do things it can't do. This capability assures, for example, that you don't ask a voltage source to slew faster than its specified maximum rate. Dantes also provides several features to aid in documenting test setups and parameters; it can accept input in the form of test schematics. Moreover, it automates the layout of test fixtures such as DUT boards.

Dantes lets you simulate these boards, including their parasitic inductances and capacitances. Thanks to the cooperation of ATE vendors, Dantes also permits simulation of the resources of mixed-signal test systems. These resources include such components as voltage/current sources, measurement subsystems, and switch matrices. Coupled with design data on the device to be tested, this simulation capability lets you accurately predict how a device will behave on a real tester.

Even after you simulate individual tests, you don't have a complete test program; you have a collection of tests. Although you might think that a test program is nothing more than such a collection, that isn't the case. Transforming the tests into a working program involves a bit of science and a bit of art. This is where tester-specific VT tools enter the picture.

Test-sequencing tools (one type of tester-specific tool) attempt to minimize test time by looking at the tester and device states at the end of each test to make sure that a minimum number of things must happen before the next test can run. Here, "things" means vectors that must be applied to the DUT or commands that must be executed to make various tester resources ready for the next test.

Even when test sequences are determined in the manner described above, throughput is not necessarily maximized. Tests that devices are most likely to fail should run first. This minimizes the time spent testing devices that will ultimately be rejected. Test-program-optimization tools attempt to strike a balance between tester- and device-state considerations and the likelihood that devices will fail individual tests.

Another part of test-program optimization is binning of devices. Binning is more of a concern with standard analog and mixed-signal parts than with most ASICs. Vendors often sort analog ICs into multiple performance grades,

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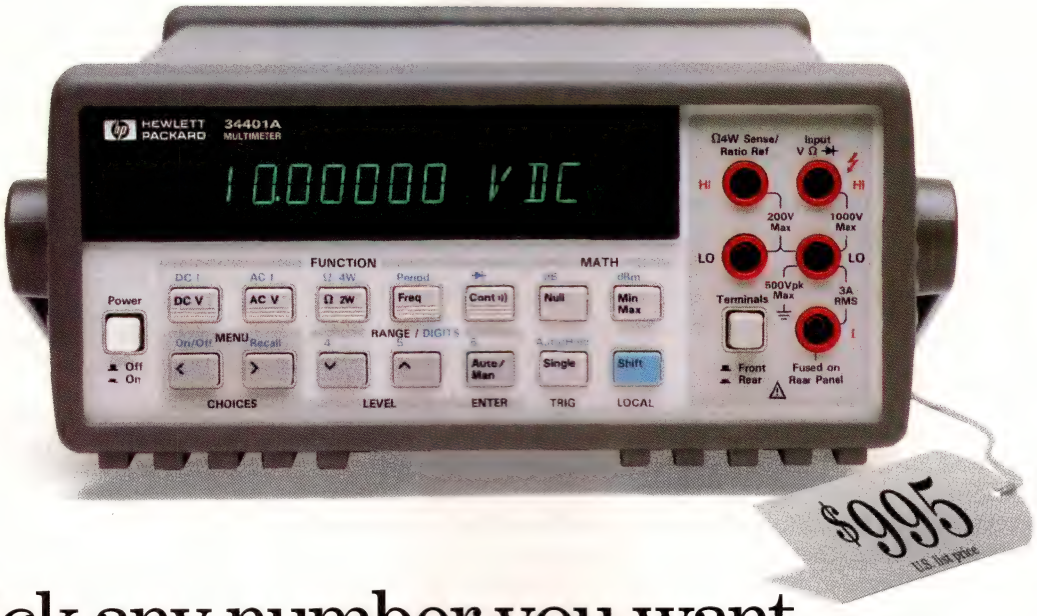

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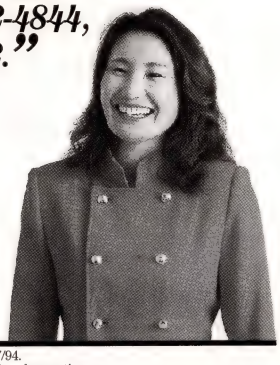

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but binning can also affect digital ICs—an example is μPs that are sorted into several speed grades. Binning strategies can influence test sequencing and throughput: You can save time when devices placed in lower performance categories need not undergo all tests.

A device can fail a test because the device is bad or because of problems with the test or the test program. Test-debugging tools provide visibility of the state of the tester, its individual resources, and, sometimes, the DUT itself to aid in determining what has gone wrong when the test results do not agree with the expected results.

Some observers of the IC-design scene comment that the role of the test engineer is becoming superfluous or that modern EDA tools are reducing the role of the test engineer to that of a technician. That is not the case. In reality, test engineers are design engineers. Instead of designing products, they design the fixtures, test programs, and processes that make possible the economical, high-quality manufacture of products thought up by design engineers. New TDA tools offer test engineers power similar to the power that EDA tools place in the hands of design engineers. But for companies to derive the full benefit of TDA, design engineers must develop more understanding of the evolving role of test engineering. And, most important, partnering between design and test must begin very early in the life of each project. EDN

Motorola's PowerPC 603 μP has approximately 300,000 gates. Thanks to structured DFT methodologies, developing test vectors for the chip was not the big job you might think. Using tools from Mentor Graphics, Motorola engineers did the job in only a few days.

Reference

1. Maxwell, Peter C, R Aitken, V Johansen, and I Chiang, "The effectiveness of IDDQ, functional, and scan tests: How much fault coverage do we need?" *Proceedings of the International Test Conference 1992,* pg 168.

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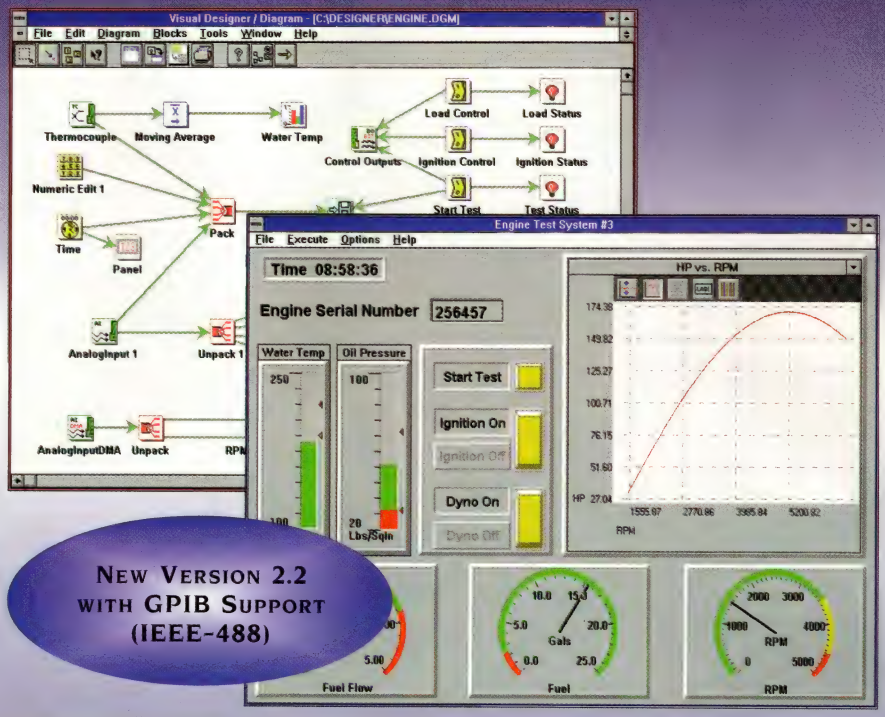

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- *Data Acquisition at Full Hardware Speeds*
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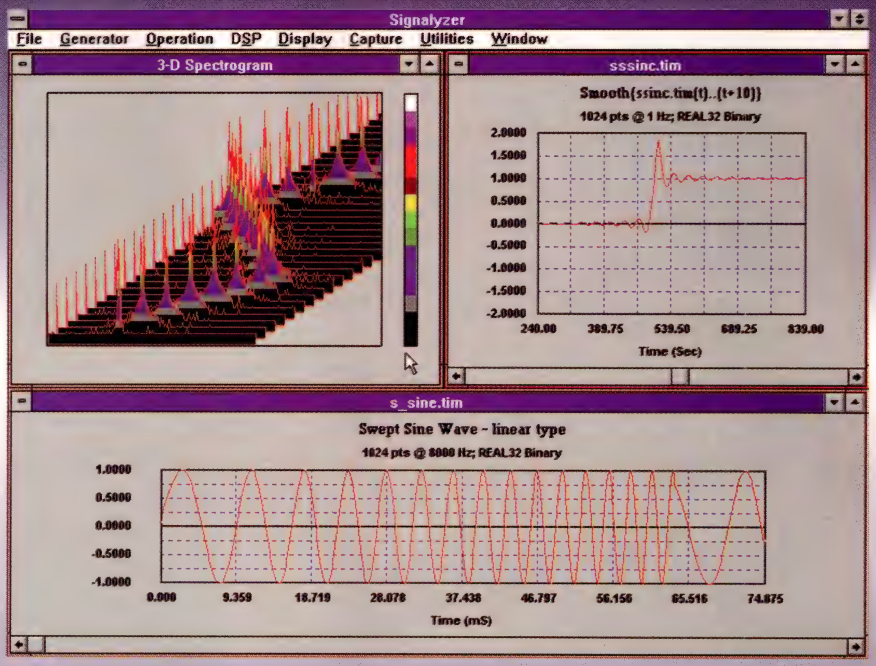


CIRCLE NO. 191

SIGNALYZER

Signalyzer, a Windows-based software package, provides a powerful tool for analyzing signals. Data acquisition can be as simple as selecting the Capture menu and specifying the setup in a dialog box. You can select channel(s), gain, sample frequency, and the amount of data to be captured. Simple menu selections allow you to manipulate, analyze, display, and/or export captured data.

Signalyzer's rich set of signal analysis functions supports both time- and frequency-domain signal analysis. Display capabilities include static displays of captured data as well as real-time oscilloscope and spectrum displays.

When used with the optional Digital Filter Design software, Signalyzer filters data files with FIR and IIR digital filters. This option generates the necessary filter coefficient files for low-pass, high-pass, band-pass and band-rejection filters.

FUNCTIONS

DISPLAYS
- Waveform
- Oscilloscope
- Spectral (1D, 2D, & 3D)
- Cursor Readouts
- Zoom
- Pan
- Autoscale
- Color Selection

ANALYSIS
- Digital Filtering
- Convolution
- Auto Correlation
- Cross Correlation
- Decimation
- Interpolation
- FFT and Inverse FFT

DATA MANIPULATION
- Add
- Subtract
- Multiply
- 1/X
- Square
- Square Root
- Shift
- Flip
- Join
- Sin(x)
- Cos(x)
- Atan(x)
- Exponential
- Extract
- Smooth
- Sample & Hold
- Quantize
- Statistics

WAVEFORM GENERATORS
- Sinusoidal
- Swept Sine
- Square
- Triangular
- Exponential
- Windowing Functions
- Unit Step
- Sinc
- Ramp
- Unit Sample
- Noise

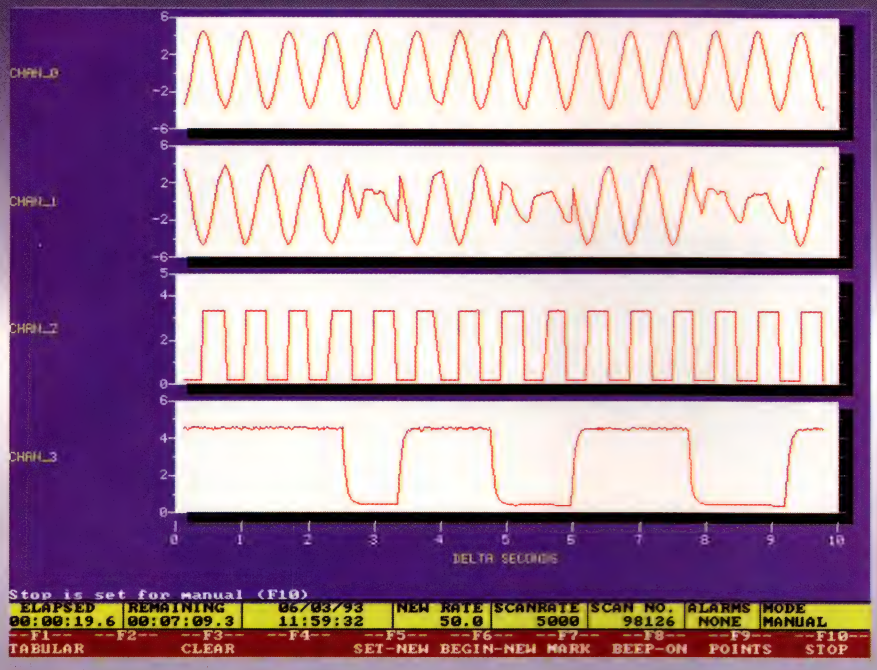
ORDERING INFORMATION

DESCRIPTION	PART NUMBER	PRICE
Signalyzer Data Acquisition, Analysis and Display Software	PCI-20395S-1	$495
Digital Filter Design Software Option	PCI-20396S-1	$295

NOTE: SIGNALYZER SUPPORTS THE PCI-20098C, PCI-20377W, PCI-20428W-1&-2, PCI-20501C AND ZPB34A BOARDS.

CHARTSTREAM

STREAM MULTICHANNEL DATA TO DISK WITH ANALYSIS AND DISPLAY



FEATURES/BENEFITS

- *Records up to 80 analog channels with real-time display*
- *Streams to disk at up to 100kHz; to memory at up to 1MHz*
- *Mathematical operations on waveforms, including integration, differentiation, and inter-channel arithmetic*
- *Graphical post-process analysis and display*
- *Graphical user interface; menu-driven operation*
- *Real-time engineering unit conversion*
- *Multiple real-time display pages*
- *Pre- and post-triggered operation*

CIRCLE NO. 192

ChartStream allows your PC to acquire, display, and analyze analog data from multiple channels without writing custom software. It is modeled along the lines of the familiar standalone chart recorder. ChartStream's two software components, the data recorder and the post-process data analyzer, operate together seamlessly.

The ChartStream Recorder streams up to 80 channels of analog data to disk at a total rate of up to 100,000 samples/second. As data is streamed continuously to disk, it is also immediately displayed on the screen in strip-chart or x-y plots or in tabular form.

ChartStream Analyzer is a powerful, yet easy-to-use, graphical data analysis package for data manipulation and display. Available graph types include strip-chart, X-Y plot, and multi-plot graphs. ChartStream also supports integrals, derivatives and three levels of smoothing.

FUNCTIONS

CHARTSTREAM RECORDER

ACQUISITION
- Up to 80 Analog Inputs
- 100kHz Stream to Disk
- 1MHz Stream to Memory
- Variable Scan Rate

TRIGGERING
- Analog Channel
- Digital Channel
- Pre- and Post-Triggered Operation

REAL-TIME CALCULATIONS
- Add, Subtract, Multiply, Divide
- Sin( )
- Cos ( )
- Tan ( )
- ASin ( )
- ACos ( )
- ATan ( )
- Abs ( )
- Ln ( )
- Log ( )
- Engineering Units
- Calculated Channels

DISPLAY
- Strip-Chart Plots
- Real-Time Display
- 10 Display Pages
- X-Y Plots
- Tabular Display

CHARTSTREAM ANALYZER
- Pan
- Zoom
- Playback
- d/dt
- ∫dt
- Smoothing
- Titles
- Labels
- Text
- Print

CHARTSTREAM

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	PRICE
ChartStream Recorder/Analyzer	PCI-20379S-1	$595

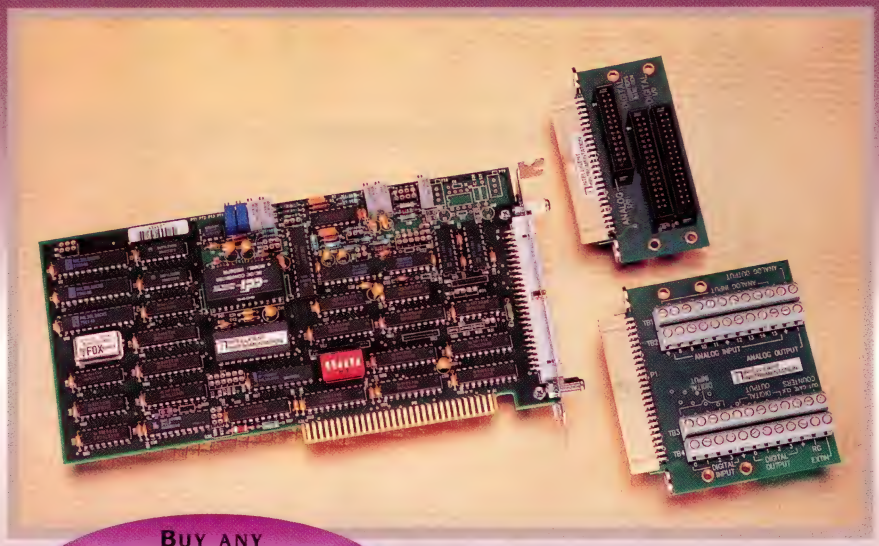
NOTE: CHARTSTREAM SUPPORTS THE PCI-20098C, PCI-20377W-1 AND PCI-20501C BOARDS.

LOW-COST DATA ACQUISITION BOARDS

PCI-20428W SERIES

FEATURES/BENEFITS

- *Premium Functionality at Low Cost*
- *100kHz Multichannel Analog I/O Throughput*
- *16SE/8Diff Analog Inputs (-3, 16SE)*
- *12-Bit Resolution*
- *DMA Data Transfer to Host Memory (External Triggering)*
- *Two 12-Bit Analog Outputs (-1 and -2 only)*
- *Dual DMA for simultaneous analog input/output*
- *8 Digital Inputs, 8 Digital Outputs*
- *1 Counter/Timer, 2 Rate Generators*
- *Includes Master Link, C Language, DOS Drivers and Windows DLL*
- ***Lifetime Warranty***



BUY ANY PCI-20428K & VISUAL DESIGNER BY DEC. 30TH '94 FOR ONLY $995 (SAVE $455)

CIRCLE NO. 193

SOFTWARE SUPPORTED:

VISUAL DESIGNER

SIGNALYZER

MASTER LINK DRIVERS

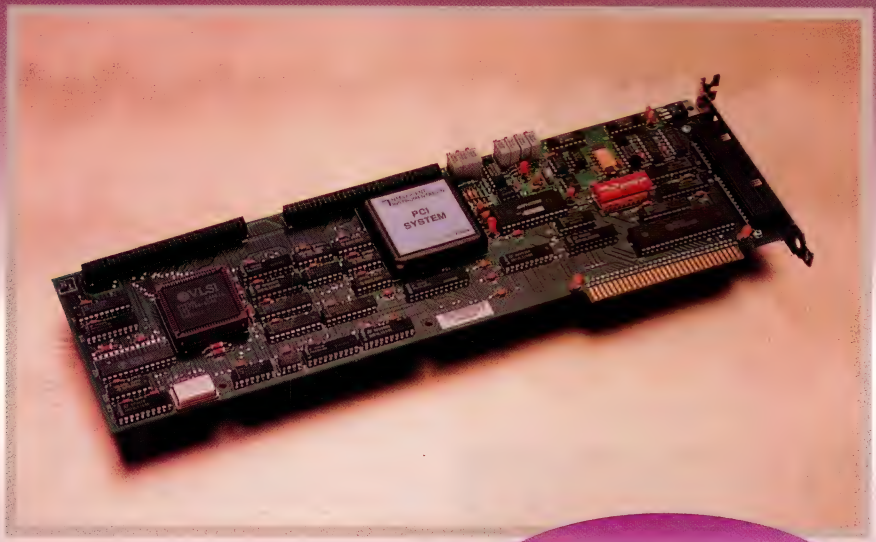
PARAMETER	CONDITIONS	SPECIFICATION
ANALOG INPUTS		
Number of Channels, Resolution	Single-ended/Differential	16/8, 12 bit
A/D Voltage Ranges		0-5V, 0-10V, ±5V, ±10V
Over Voltage	Power On/Off	±35V/±20V
Common Mode Rejection	60Hz, 100 Ohm Unbalance, Gain 100	-92dB (0.05lsb/V)
Linearity Error		±0.024%FS
Throughput, Multichannel	DMA, Triggered DMA	100kHz
ANALOG OUTPUTS (-1 & -2 only)		
Channels, Resolution		2, 12 bits (1 part in 4096)
Voltage Ranges		0-10V, ±5V, ±10V
Throughput	Using DMA	100kHz
DIGITAL I/O		
Number of Ports, Levels		2 (1 input, 1 output), TTL
COUNTER		
Number of Channels, Clock Speed		1 (16 bit), 8MHz
POWER REQUIREMENTS	+5V	1A

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	PRICE
Low-cost I/O Board (Gain 1, 10, 100)	PCI-20428W-1	$395
Low-cost I/O Board (Gain 1, 2, 4, 8)	PCI-20428W-2	$395
Low-cost I/O Board (Gain 1, without Analog Outputs)	PCI-20428W-3	$295
Low-Cost I/O Board (Gain 1, 10, 100) with Termination Panel	PCI-20428K-1	$455
Low-Cost I/O Board (Gain 1, 2, 4, 8) with Termination Panel	PCI-20428K-2	$455
Low-Cost I/O Board (Gain 1, without Analog Outputs) with Termination Panel	PCI-20428K-3	$355

EXPANDABLE DATA ACQUISITION BOARDS

PCI-20098C SERIES



FEATURES/BENEFITS

- *Completely Software Programmable*
- *Up to 100kHz Multichannel Gap-Free Sampling*
- *16SE/8Diff 12-bit Analog Inputs*
- *Random Channel/Gain Sequencing*
- *DMA, Interrupt and Polled Modes*
- *Burst-Mode Sampling, Triggering*
- *16 Buffered Digital I/O Channels*
- *Two 16-Bit Counters*
- *Accepts up to Two Option Modules*
- *Includes Master Link Software Drivers for DOS and Windows*
- ***Lifetime Warranty***

CIRCLE NO. 194

BUY ANY PCI-20098C & VISUAL DESIGNER BY DEC. 30TH '94 AND SAVE $400

PARAMETER	CONDITIONS	SPECIFICATION
ANALOG INPUTS		
Number of Channels, Resolution	Single-ended/Differential	16/8, 12 bit (1 part in 4096)
Channel Expansion	Using Option Modules	to 80 SE, to 40 Diff
A/D Voltage Ranges		0-10V, ±5V, ±10V
Software Programmable Gains		1, 10, 100, 200
Over Voltage	Power On/Off	±35V, ±20V
Common Mode Rejection	60Hz, 100 Ohm Unbalance, Gain 200	90dB (0.05lsb/V)
Linearity Error		±0.012%FS
Throughput, Multichannel w/ DMA	PCI-20098C-1, -2 Gain 1,10	45KHz, 100KHz
DIGITAL I/O		
Number of Ports, Levels	Programmable	2 (expandable to 8), TTL
COUNTERS		
Channels, Clock Speed, Levels	Maximum	2, 16MHz, TTL
BURST GENERATOR		
Range, Resolution, Level		0.002Hz to 2MHz, 125ns, TTL
POWER REQUIREMENTS	+5V	1.7A Max

SOFTWARE SUPPORTED:

VISUAL DESIGNER

SIGNALYZER

CHARTSTREAM

MASTER LINK DRIVERS

EXPANSION MODULES			
PCI-20031M-1	32SE, 16 Diff Analog Expander	PCI-20003M-2	2 Ch., 12-bit Analog Output
PCI-20363M-2	8 Chan., Simultaneous Sample/Hold, Expander	PCI-20006M-2	2 Ch., 16-bit Analog Output
PCI-20020M-1	Analog Trigger/Alarm	PCI-20021M-1B	8 Ch., 12-bit Analog Output
		PCI-20004M-1	32 Ch., Digital I/O

ORDERING INFORMATION

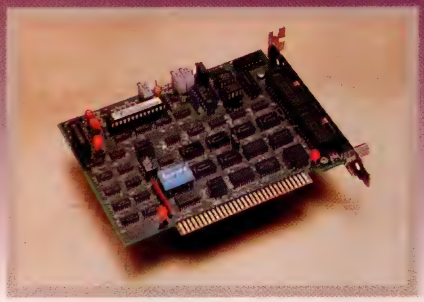
DESCRIPTION	PART NUMBER	PRICE	PRICE WITH VISUAL DESIGNER
Expandable 1/0 Board; 45kHz	PCI-20098C-1	$795	$1390
Expandable 1/0 Board; 100kHz	PCI-20098C-2	$895	$1490
Expandable 1/0 Board; 45kHz with Termination Panel & Cables	PCI-20098K-1	$1150	$1745
Expandable 1/0 Board; 100kHz with Termination Panel & Cables	PCI-20098K-2	$1250	$1845

Low-Power Data Acquisition Boards

PCI-20377W Series

FEATURES/BENEFITS

- 45kHz and 100kHz Models, 12-Bit Resolution
- 16 SE/8 Diff Analog Inputs with DMA Data Transfer to Host Memory
- Rate Generator with 8MHz Crystal Timebase
- DMA Data Transfer to Host
- 8 Digital Input, 8 Digital Output Channels
- Two 16-Bit Counters
- Includes Master Link Software Drivers for DOS and Windows
- **Lifetime Warranty**



CIRCLE NO. 195

SOFTWARE SUPPORTED:

VISUAL DESIGNER | CHARTSTREAM | SIGNALYZER | MASTER LINK DRIVERS

PARAMETER	CONDITIONS	SPECIFICATION
ANALOG INPUT		
Number of Channels, Resolution	Single-ended/Differential	16/8, 12-bit (1part in 4096)
A/D Voltage Ranges		0-10V, ±5V
Software Programmable Gains		1, 10, 100, 200
OverVoltage	Power On/Off	±35V, ±20V
Common Mode Rejection	60Hz, 100 Ohm Unbalance, Gain 200	90db, (0.05lsb/V)
Linearity Error		±0.012%FS
Throughput, Multichannel w/ DMA	PCI-20377W, -2 Gain 1, 10	45KHz, 100KHz
DIGITAL I/O		
Number of Ports, Levels	Programmable	2 (1 input, 1 output), TTL
COUNTERS		
Channels, Clock Speed, Levels		2, 8MHz, TTL
RATE GENERATOR		
Range, Resolution, Level		0.002Hz to 2MHz, 125ns, TTL
POWER REQUIREMENTS	+5V	300mA, 1.5W

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	PRICE
Low-Power I/O Board; 45kHz	PCI-20377W-1	$495
Low-Power I/O Board; 100kHz	PCI-20377W-2	$545
Low-Power I/O Board; 45kHz, with Termination Panel & Cables	PCI-20377K-1	$815
Low-Power I/O Board; 100kHz, with Termination Panel & Cables	PCI-20377K-2	$865

1MHz Expan

PCI-205

FEATURES/BENEFITS

- Completely Software Programmable
- 1MHz Gap-Free Throughput To Host Memory
- 8SE, 12-Bit Analog Inputs
- Two DMA Channels
- Random Channel Sequencing
- Burst-Mode Sampling, Triggering
- 16 Digital I/O Channels
- Two 16-Bit Counters
- Accepts up to Two Option Modules
- Includes Master Link Software Drivers for DOS and Windows
- **Lifetime Warranty**

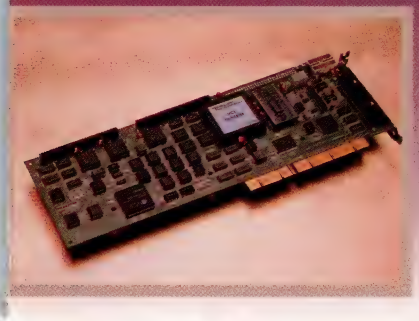
PARAMETER	CONDITION
ANALOG INPUTS	
Number of Channels, Resolution	Single-ended (PCI-20
Channel Expansion	Using Option Modules
A/D Voltage Ranges	
OverVoltage	Power On/Off
Linearity Error	
Throughput, Multichannel w/ DMA	PCI-20501C-1
DIGITAL I/O	
Number of Ports, Levels	Programmable
Throughput w/ DMA	
COUNTERS	
Channels, Clock Speed, Levels	
BURST GENERATOR	
Range, Resolution, Level	
POWER REQUIREMENTS	+5V

EXPANSION MODULES (EISA)	
PCI-20368M-1	16 Ch. Analog Expander
PCI-20363M-2	8 Ch. Simultaneous Sample/Hold Expa
PCI-20020M-1	Analog Trigger/Alarm

ORDERING INFORMATION

DESCRIPTION
1MHz 1/0 Board for EISA computers
1MHz 1/0 Board for EISA computers with Termination Panel & Cables

BLE BOARD
C SERIES



CIRCLE NO. 196

SOFTWARE SUPPORTED:

VISUAL DESIGNER | CHARTSTREAM | SIGNALYZER | MASTER LINK DRIVERS

	SPECIFICATION
C-1 only)	8, 12 bit (1 part in 4096) to 40 SE 0-10V, ±5V ±35V, ±20V ±0.036% FS 1MHz
	2 (expandable to 6), TTL 1 Mbyte/sec
	2, 16MHz, TTL
	0.002Hz to 2MHz, 125ns, TTL
	3.7A Max

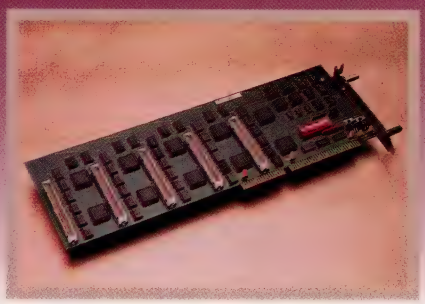
der	PCI-20003M-2	2 Ch., 12-bit Analog Output
	PCI-20006M-2	2 Ch., 16-bit Analog Output
	PCI-20021M-1B	8 Ch., 12-bit Analog Output
	PCI-20004M-1	32 Ch. Digital I/O

PART NUMBER	PRICE
PCI-20501C-1	$2470
PCI-20501K-1	$2810

DIGITAL I/O BOARDS
PCI-20378W AND PCI-20087W SERIES

FEATURES/BENEFITS

- 40, 120 or 240 Digital I/O Channels
- Programmable as Inputs or Outputs in 8-Bit Ports
- Software Programmable; No Jumpers
- High Current-Sink (24mA) and Source (15mA) Capability
- Includes Master Link Software Libraries for DOS and Windows
- ***Lifetime Warranty***



CIRCLE NO. 197

SOFTWARE SUPPORTED:

VISUAL DESIGNER | MASTER LINK DRIVERS

The PCI-20378W Series and PCI-20087W-1 Digital I/O Boards interface with the expansion bus on an ISA (PC/AT or EISA) computer. The PCI-20378W-1 has 30 eight-bit-wide ports and provides 240 channels of buffered TTL I/O. The PCI-20378W-3 has 15 ports and provides 120 channels of buffered TTL I/O. And the PCI-20087W has 5 eight-bit-wide ports and provides 32 channels of buffered and 8 channels of unbuffered TTL I/O. You can program each port individually for either input or output. The buffers provide a source capability of 15mA and a sink capability of 24mA.

PARAMETER	PART NUMBER	SPECIFICATION
DIGITAL I/O		
Number of Ports	PCI-20378W-1	30
	PCI-20378W-3	15
	PCI-20087W	5 (4 full buffered)
Input Levels	All	TTL compatible
Output Current	All	Source Current Vout = high 15mA Sink Current Vout = low 24mA
INTERRUPTS		
Sources	PCI-20378W-1	Up to 6
	PCI-20378W-3	Up to 4
	PCI-20087W	Up to 3
PC Levels	All	[2 through 7]
POWER REQUIREMENTS		
	PCI-20378W-1	+5V , 3.65A maximum
	PCI-20378W-3	+5V , 2.14A maximum
	PCI-20087W	+5V , 425mA

ORDERING INFORMATION

DESCRIPTION	PART NUMBER	PRICE
240 Channel Digital I/O	PCI-20378W-1	$495
120 Channel Digital I/O	PCI-20378W-3	$349
40 Channel Digital I/O	PCI-20087W-1	$179

DSP Processor Boards

ZPB34A Series

Our DSP product line offers both fixed and floating point solutions. Our DSP boards are supported by a wide range of analog input and output options.

For more Information on our DSP Product Line (800) 685-9911

CIRCLE NO. 198

FLOATING POINT DSP BOARDS

PART NUMBER	DESCRIPTION	PRICE
ZPB34A	AT&T DSP32C, 50MHz, 64K to 2.25M RAM	from $995
ANALOG I/O OPTIONS:		
ZPB100	1ch, 16-bit, 8kHz input/output	$395
ZPD1002	2ch, 12-bit, 10MHz input	$3495
ZPD1003	1ch, 16-bit, 500kHz input	$2295
ZPD1007	2ch, 16-bit, 200kHz input/output	$1495
ZPB1008	8ch, 12-bit, 100KHz input	$1195

FIXED POINT DSP BOARDS

PART NUMBER	DESCRIPTION	PRICE
PCI-20202C	TI TMS320C25, 50 MHz, 64K RAM	from $995
EXPANSION MODULES:		
PCI-20019M-1A	8 Channel, 89kHz, 12-bit Analog Input	$560
PCI-20023M-1	8 Channel, 200kHz, 12-bit Analog Input	$895
PCI-20341M-1A	4 Channel, 85kHz, 16-bit Analog Input	$695
PCI-20003M-2	2 Channel, 12-bit Analog Output	$195
PCI-20006M-2	2 Channel, 16-bit Analog Output	$545
PCI-20021M-1B	8 Channel, 12-bit Analog Output	$570

Multibus Data Acquisition Products

Our Multibus product line offers a wide range of industrial I/O including: analog input, analog output, digital I/O and counter/timer boards.

For more Information on our Multibus Line (800) 685-9911

CIRCLE NO. 199

DIGITAL I/O AND COUNTER BOARDS

PART NUMBER	DESCRIPTION	PRICE
MP802B	32 Channel Relay Output Board (0.5A, 10W per channel)	$765
MP810NS	24 Channel Isolated Digital Input (0 to 84VDC, 0 to 168VAC)	$875
MP830-72	72 Channel Digital Input/Output	$655
MP821B-15	15 Channel Counter/Timer	$1645

ANALOG INPUT BOARDS

PART NUMBER	CHANNELS	INPUT RANGES	RESOLUTION	PGA	RATE	ANALOG OUTPUT	PRICE
MP8418B	31SE/15Diff	±2.5, 0-5, ±5 0-10, ±10 Volts	12-bits	None	26 kHz	2 ch, 12-bit	$1,315
MP8418B-PGA	31SE/15Diff	±2.5, 0-5, ±5, 0-10,±10 Volts	12-bits	1 to 1000	2.8 kHz	2 ch, 12-bit	$2,085
MP8418B-EXP	96SE/48Diff	±2.5, 0-5, ±5, 0-10,±10 Volts					$865

ANALOG OUTPUT BOARDS

PART NUMBER	CHANNELS	OUTPUT RANGES	RESOLUTION	CONVERSION TIME	PRICE
MP8316-V	16	±2.5, 0-5, ±5, 0-10, ±10 Volts	12-bit	3.5 msec	$1,095
MP8316-I	16	0-24.5 mA	12-bit	8.5 msec	$1,265

MICROTERMINALS

FOR OPERATOR INTERFACE & DATA COLLECTION

Our broad line of microterminals allows you to select a model with just the features you need—from a basic operator interface to a multifunction unit for bar code data collection. We offer a selection of cases, functions, keyboards, displays and much more.

You'll find our products in use worldwide as operator interface/control panels or as data collection terminals. Ideal applications include:

OPERATOR INTERFACE/ CONTROL PANELS

- Instrumentation
- Communications Products
- Machine Set-Up & Control
- Test and Measurement
- Process Controllers
- Inventory Control

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DATA COLLECTION TERMINALS

- Shop Floor Control
- Material Tracking
- Time & Attendance
- Inventory Control
- Quality Control
- Machine Monitoring

CIRCLE NO. 200

PARAMETER	SPECIFICATIONS
Communications	RS232, RS422
Display	1 x 16 LCD, LED or 2 x 40 Backlit LCD
Keypad	Numeric, Alphanumeric
Physical	NEMA 4 (IP66) Extended Temperature Available
Functions	6 to 18 Programmable

LANPOINT COMPUTERS

LAN-READY BAR CODE PCs

LANpoint Computers® are a family of compact, rugged DOS PCs designed to add bar code capabilities to a LAN. Both bar code decoding and an Ethernet™ interface are built-in. And a standard PC COM1 port can be used to attach serial or RS232 devices.

- LANpoint® is the smallest unit, measuring just 9.0"W x 5.0"H x 1.5"D and weighing only 1.7lb. It includes a full keyboard.
- TIMEpoint®, designed for time & attendance, features a cast-metal case and a built-in bar code or magnetic stripe reader.
- FACTORYpoint®, our NEMA 4 (IP66) industrial model, withstands the harshest environments.

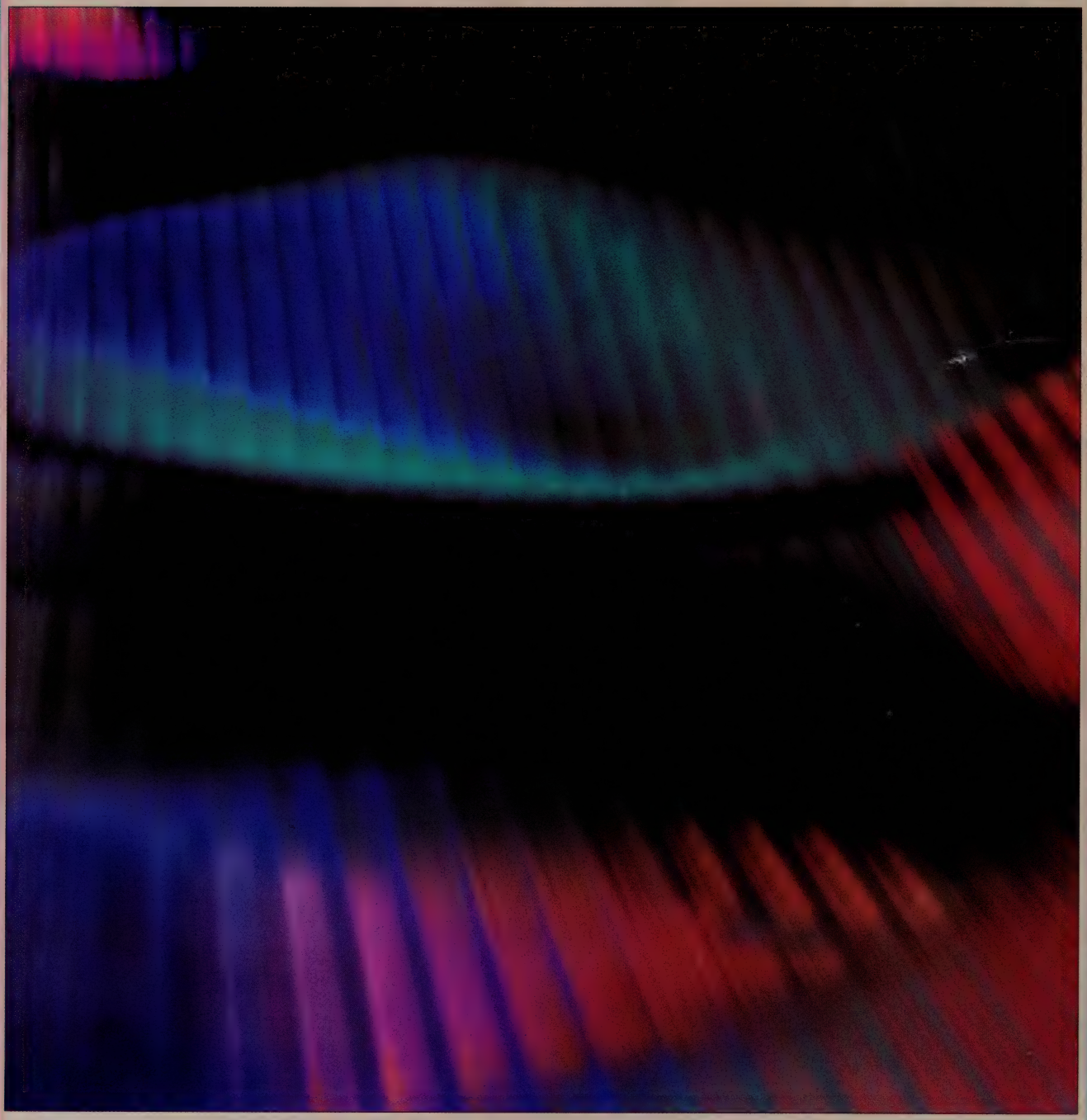
Companies worldwide count on our LANpoint Computers for applications such as:

- Material & Document Tracking
- Shipping & Receiving
- Time & Attendance
- Job Costing
- Labor Data Collection

yes NetWare Tested and Approved

FOR COMPLETE LANPOINT INFORMATION
(800) 685-9911

CIRCLE NO. 201



INTELLIGENT INSTRUMENTATION™

A Burr-Brown Company

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BLI-186

Printed in the USA, *August* 1994

How to Get a Benchful of Signals Without a Bench Full of Generators.

Gone are the days of scouring the lab for function-specific generators.

At a price that's less than many single-purpose generators, Wavetek's new Model 395 does the job of seven different signal sources and does every job extremely well.

In an instant you can choose from a host of signals, from clean sine waves up to 40 MHz to complex pulse trains and arbitrary waveforms. When you use Model 395 as a pulse generator, for example, you can individually control the amplitudes, widths, and rise and fall times for up to ten pulses in a train. On-screen help makes signal selection easier than ever.

Take your choice: function generator, sweep generator, pulse generator, modulator, trigger generator, noise generator, arb, and all of the above.

You can create many signals that might otherwise require hooking together two, three or more generators. With gating, looping, linking, signal summing, and complete arbitrary waveform capability, our universal signal source can produce just about any waveform you can conceive. You can even store any setup for later use – for recall at the touch of a button!

So come to the source for all your signal needs. Call Wavetek today at **1-800-223-9885**, and get all the details on the new Model 395 universal signal source.

The Universal Signal Source.

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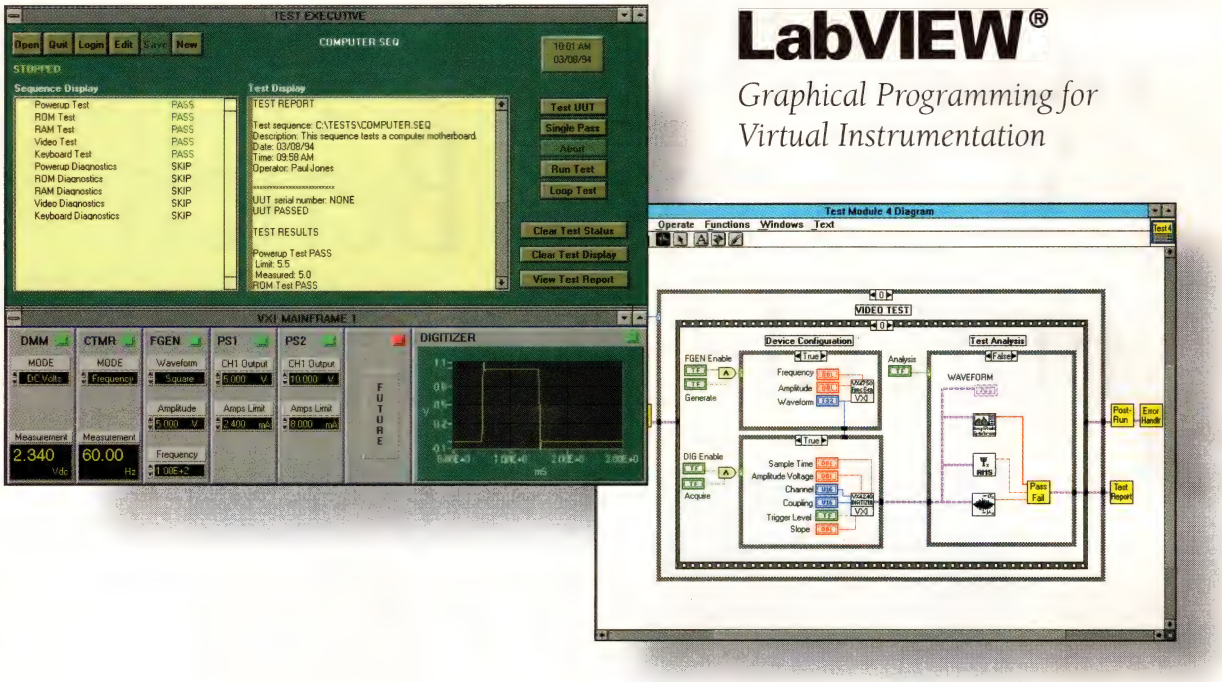
CIRCLE NO. 97

WAVETEK

What's Revolutionizing the Test Industr



LabVIEW®

Graphical Programming for Virtual Instrumentation

Virtual Instru

A True Breakthrough in Instrumentation

Virtual Instrumentation is revolutionizing the test industry. How? By empowering you to build your test systems better than ever before. Reusing both hardware and software from one system to the next. Easily enhancing existing systems to meet future needs. Using your existing instruments and even leveraging your existing code. Most importantly, doing all this in less time and for less money using industry-standard computers and object-oriented software.

A True Breakthrough in Productivity

Virtual instrumentation is much more than a graphical user interface or a layer of icons in the name of "ease of use" – it's a new philosophy. A philosophy that delivers a true breakthrough in efficiency and productivity. Where software is optimized for you and by you. Where both hardware and software are open, modular, reusable, and interchangeable. Where vendor-defined becomes user-defined through flexible software combined with general-purpose instruments.

A True Breakthrough in Software

At National Instruments we understand the importance of software for virtual instrumentation. That's why we've pioneered this revolution with the test industry's two leading software products.

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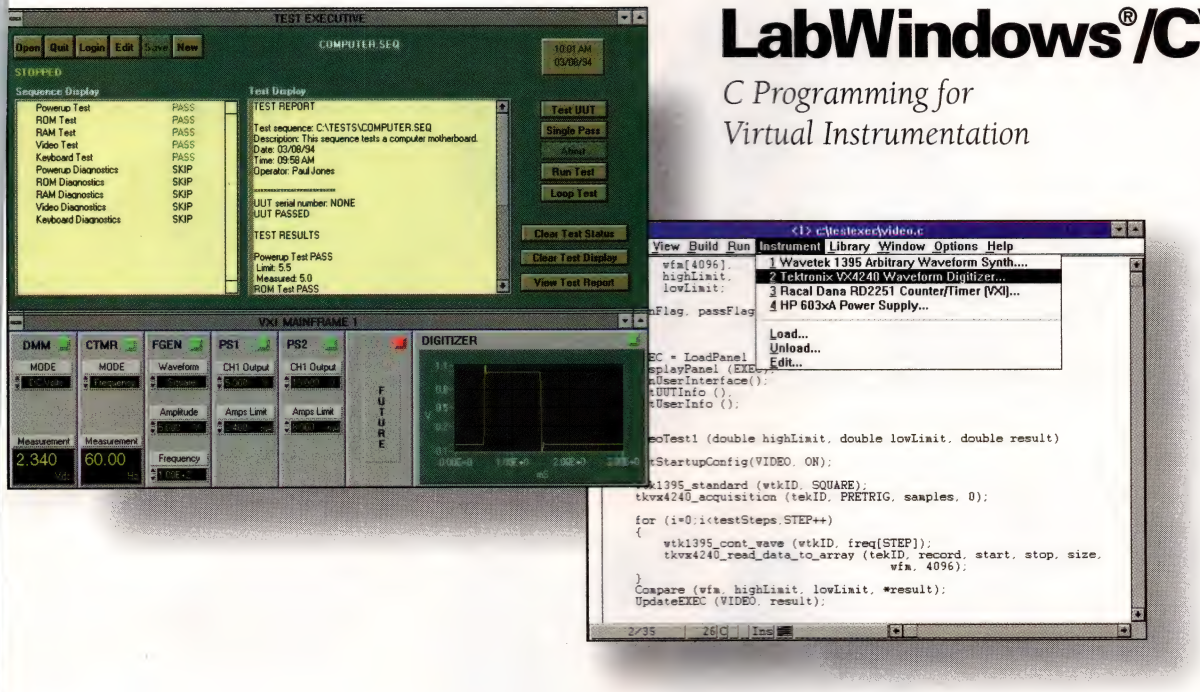

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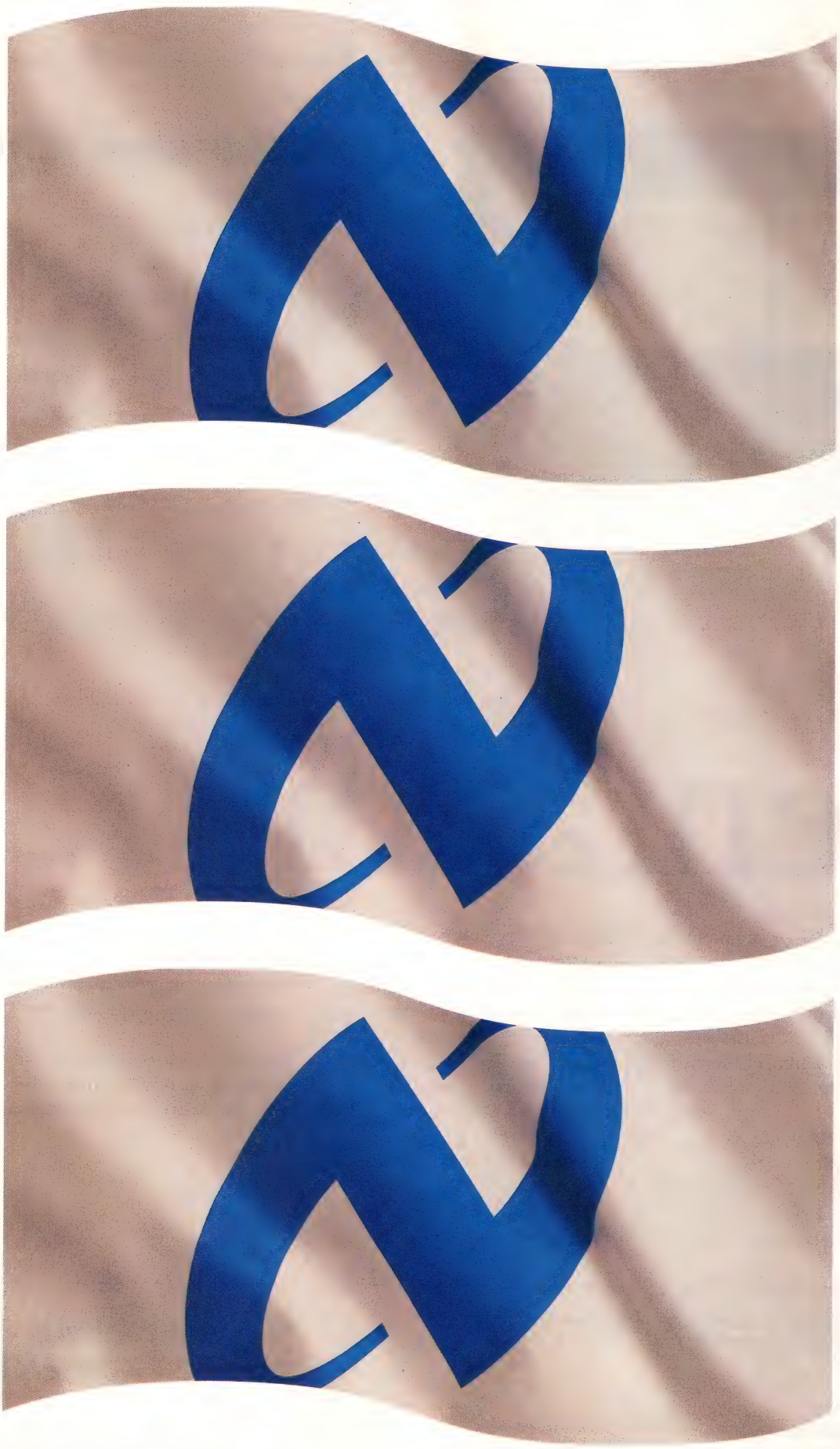

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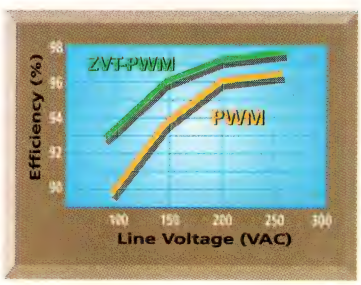

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CIRCLE NO. 46

Evolving ADCs DEMAND MORE from drive amplifiers

ANNE WATSON SWAGER, TECHNICAL EDITOR

FINDING AN AMPLIFIER THAT DOESN'T TARNISH AN ADC'S PERFORMANCE IS HARD ENOUGH. BUT NOW YOU ALSO HAVE TO DEAL WITH SINGLE-SUPPLY VOLTAGES AND THE QUIRKY SWITCHED-CAPACITOR INPUT STRUCTURE.

OP-AMP DESIGNERS ARE scrambling to keep pace with changes in ADCs, changes that often make driving these converters more difficult. Ever-increasing speed and resolution, more ADCs with single-supply voltages, and more ADCs with switched-capacitor input structures are forcing system designers to carefully evaluate the drive amplifier's performance.

Depending on the input signal and source, many sampling A/D converters—particularly the switched-capacitor types—require an input-drive amplifier to amplify extremely low-level signals, to provide a low-impedance source for the ADC inputs, or to provide the necessary drive current for the ADC.

You might ask why manufacturers of monolithic, hybrid, and modular products don't routinely include op amps or buffers in front of their ADCs. In the case of an IC, ADC manufacturers use processes that may not be compatible with drive-amplifier requirements. For example, using a CMOS process makes it difficult to meet the low-drift and -noise requirements of high-performance analog functions. In the case of hybrid and modular ADCs that combine high resolution and speed, manufacturers don't include amplifiers because applications often require different amplifiers, such as one optimized for low noise or another optimized for low distortion.

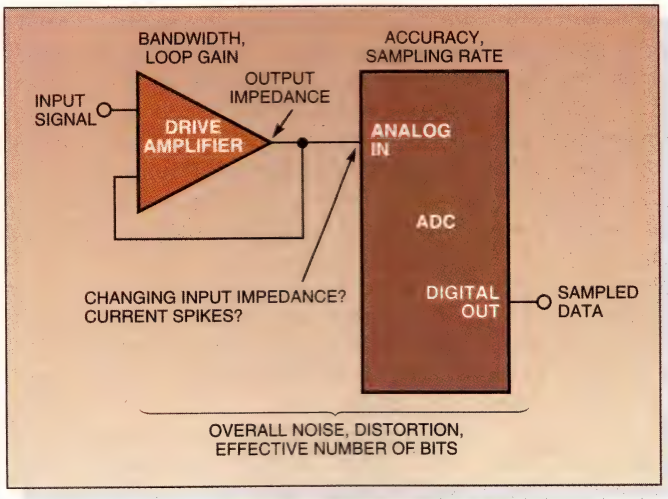
ADC manufacturers, particularly those that also produce op amps, often make specific drive-amplifier suggestions. However, the drive amp you ultimately choose needs to closely match your system requirements. Choosing the optimum drive amplifier requires looking at the problem from two perspectives. The first is sheer overall performance. The second is the specific ADC input structure and how it can affect the performance of the op amp.

To provide the best overall performance, the op amp ideally should contribute no additional error to that of the ADC. One way to ensure this is to use an amplifier whose noise, as measured in S/N ratio, is much better than the ADC's theoretical, best-case dynamic range. The familiar equation for this range is:

$$6.02 \times N + 1.76 \text{ dB},$$

where N equals the number of bits. For a 12-bit system, then, an amplifier should have an S/N ratio of 74 dB.

Willie Rempfer, design manager of ADCs at Linear Technology, recommends that you also keep in mind the results of adding the noise power of two sources—in this case, the op amp and the ADC. A simple calculation tells you what the combined S/N ratio is. First, transform the



Choosing the best amplifier for driving an ADC requires that you evaluate the amplifier from two perspectives. First, you must ensure overall op-amp and ADC performance. Second, you must examine your ADC's input structure and take steps to minimize its effect on the amplifier.

DRIVE AMPLIFIERS FOR ADCs

S/N ratios in –dB to voltages, that is, divide by 20, then calculate 10^x. Next, calculate the square root of the sum of the squares and then convert the result back to dB by multiplying the log by 20.

The results from a series of these calculations demonstrates how an op amp can affect the overall performance. For two components with equal S/N ratios, say 93 dB, the joint S/N ratio is 3 dB less at 90 dB. If you choose an op amp with an S/N ratio 3 dB higher than that of the ADC, you knock the overall S/N ratio down by only 1.8 to 91.2 dB. With a 6-dB difference, an ADC of 93 dB and an op amp of 99 dB produce an overall result 1 dB down, or at 92 dB. A difference of 10 dB produces an almost-negligible difference—0.4 dB.

The point of these theoretical calculations is that the op amp has to be much have a higher S/N ratio than the ADC to have no detrimental effect on the ADC's performance.

Another way to evaluate op amps, suggest Texas Instruments engineers Al Miller and Paul Nossaman, is to compare an op amp's performance to the weight of an ADC's LSB in volts. For example, the LSB weight of a 10-bit converter with a 4V input range is 3.9 mV (4V/1024). Compare this number to amplifier specifications, such as input-offset voltage, drift, and noise, all multiplied by the closed-loop gain, to get an idea of the errors the amplifier introduces. For example, an amplifier with a gain of 10 multiplied by an offset of 0.5 mV produces 5 mV, or 1.28 LSBs, of error.

Bandwidth, settling time

To determine the speed requirements of a drive amplifier, you need to match the amplifier's settling time to the ADC's acquisition time. Also, bandwidth requirements can be much more than you expect. Burr-Brown Applications Manager Bonnie Baker says that many customers drastically underestimate the bandwidth necessary to sustain gain accuracy. Without substantial amounts of gain over the input signal bandwidth, you can easily introduce errors that exceed 1 LSB.

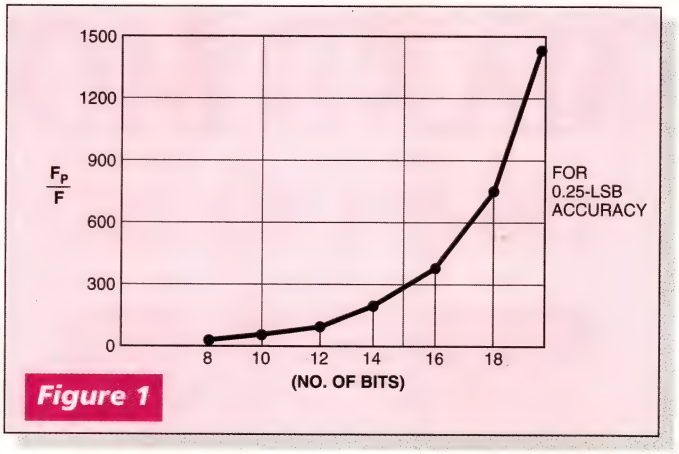


Figure 1

This plot for a theoretical, single-pole system provides an idea of the relationship between the input signal's frequency and a dominant, single-pole frequency to produce a given level of accuracy. For 12-bit single-pole systems, the single-pole frequency F_p must be 100 times the signal frequency F to introduce no gain errors. (Courtesy Burr-Brown Corp)

Fig 1, which applies only for single-pole systems and for accuracy of 0.25 LSB, provides a general idea of how high a single-pole frequency must be to produce a particular level of accuracy. For example, consider a unity-gain amplifier with a single closed-loop pole at 10 MHz (F_p=10 MHz). According to the plot, the highest signal frequency (F) you can amplify to 12-bit accuracy is 100 kHz because F_p/F is approximately equal to ≈100 at 12 bits. Worse yet, for 16-bit accuracy, the plot indicates that you would need almost 400 times greater amplifier closed-loop bandwidth than signal bandwidth. (Remember, amplifiers can have more than one pole, the pole of the amplifier may not be the dominant pole, and the plot applies to 0.25 LSB accuracy. The graphs for 0.5 and 1 LSB accuracy would be flatter.)

Certain applications require amplifiers with higher performance levels than those that the ADC typically dictates. Undersampling, for example, requires that an amplifier's bandwidth be compatible with the high-frequency input signal, not the slower sampling rate of the ADC.

After defining your requirements, you hope to find an amplifier that meets those specifications. Unfortunately, this may not be easy. Engineers at Analogic and Datel know all too well that the choice of ADCs to drive the companies' high-resolution and high-speed ADCs (**Ref 1**) is limited. Although numerous suitable op amps are available for 12-bit ADCs, only a handful of parts is suitable for driving the 14- and 16-bit, above-500-kHz, hybrid and modular ADCs that these companies produce. According to Don Travers, Analogic's product marketing manager, engineers at Analogic can spend as much time working on the front end as on the ADC itself.

When recommending op amps to their customers, both of these companies choose from a select group. Depending on the applications, the choice requires a tradeoff between distortion, noise, and settling time. Settling time is particularly difficult because few manufacturers test to a settling time of 0.001% that's approximately equivalent to 16-bit performance.

For example, Analogic recommends Analog Devices' AD843 ($3.70) (all prices quoted are for 1000-piece quantities) for applications requiring the fastest settling, but this choice doesn't result in the lowest noise performance. For lowest distortion, they recommend the AD845 ($2.76). Datel engineers also recommend the AD845, which, according to the company's tests, settles to 14-bit accuracy in 400 to 500 nsec. The AD811 ($2.85) has even faster settling to 14 bits, or 200 nsec. Even faster is Comlinear's CLC402 ($5.25), which for 2V signals settles to 14-bit accuracy in 50 nsec. Burr-Brown's OPA627 ($7.35), which is somewhat slower but accurate to 14 bits, also makes Datel's recommended list.

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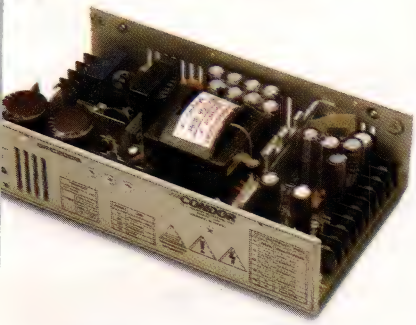

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CIRCLE NO. 64

DRIVE AMPLIFIERS FOR ADCs

amplifiers, the AD9631 and AD9632 (both $4.12). At 1 and 5 MHz, respectively, these amplifiers exhibit typical distortion of -113 and -95 dBc. Spectral noise density is 7 nV $\sqrt{Hz}$. Settling time to 0.01% is typically 16 nsec.

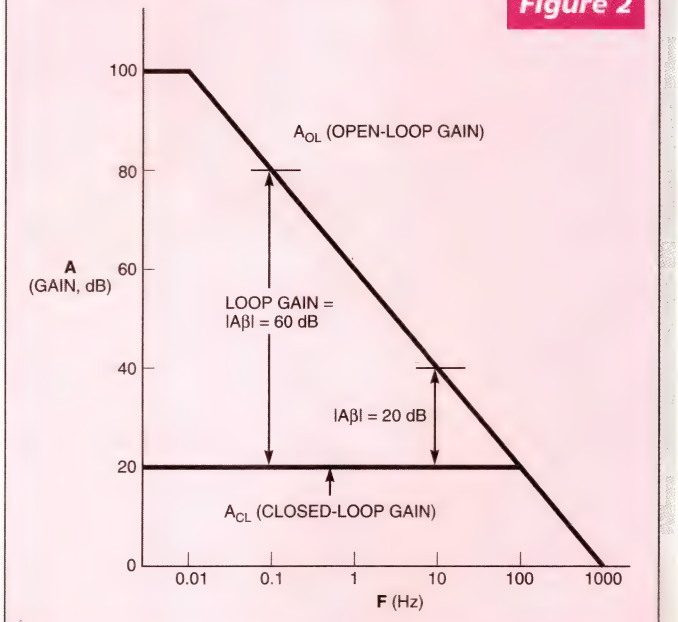
Lower input ranges

The group of high-accuracy and high-speed amplifiers starts to dwindle as power-supply voltages decrease. The current crop of 14- and 16-bit ADCs with sampling rates of 1 MHz and above typically have wide input ranges of±5 or±10V and work from high supply voltages of ±15V and sometimes an additional +5 or –5V supply. However, these companies are considering designing lower voltage parts that might present a problem in accuracy rather than speed. For example, Analogic designer Tony Dicicco knows of no amplifier that settles to 16-bit level without a thermal tail in the ±5V amplifier supply range.

Supply voltage has a decided impact on amplifier performance. Numerous amplifiers can meet 12-bit accuracy and distortion specs at 1 MHz, but few can do this while operating from a single 5V supply. Although many companies have already announced numerous single-supply amplifiers—at the latest count, Analog Devices has 11 families and 25 products—most are still designing op amps that can drive the higher performance, single-supply ADCs.

Designing an amplifier with wide input and output ranges and other characteristics, such as low distortion, wide bandwidth, fast settling, and capacitive drive, is no easy task. According to Walt Kester, staff applications engineer with Analog Devices, an op amp doesn't have to be rail-to-rail on both the inputs and outputs. In general, it's more important for an op amp to have an input that can go to ground than one whose input can go to the positive rail. Another important asset of an amplifier is that its output swing within $V_{CE(SAT)}$ of either supply rail, which implies common-emitter or totem-pole outputs instead of the traditional emitter-follower outputs.

Figure 2



The classic open- and closed-loop curves show that loop-gain—which is inversely proportional to output impedance—decreases as you approach the unity-gain crossover frequency. The higher the output impedance, the more difficulty an amplifier has handling current spikes from the ADC.

To achieve higher ac performance for their single-supply amplifiers, companies are designing new input and output stages. For the new OP279 ($1.31), designers at Analog Devices altered the usual input biasing to reduce distortion. The amplifier can typically supply±80 mA and has a THD specification of 0.01%. A patent-pending output stage in Maxim Integrated Products' MAX492 ($2.25) and MAX493 (from $1.45) family helps these rail-to-rail output amps drive capacitive loads. Maxim recommends the 500-kHz MAX492 family for driving ADCs, such as the company's 12-bit, 75k-sample/sec MAX187.

Still, single-supply op amps have a long way to go before they can adequately drive 16-bit ADCs or those faster than 1 MHz. For example, the current crop of single-supply amplifiers cannot meet the noise or open-loop gain requirements for driving 16-bit delta-sigma ADCs.

On the high-speed side, National Semiconductor is working to design a better amplifier to drive its 12-bit, 1-MHz ADC12062 ADC. Finding an amplifier that swings 5V rail-to-rail at this speed is difficult. Until the last few months, the company recommended its LM6361 ($1.75) amplifier, which requires bipolar supplies. However, the company recently announced the rail-to-rail LM6142 ($2.10). Compared with driving the 12062 with a perfect source, driving the ADC with the 6142 reduces S/N ratio plus distortion by just 1 dB, from 70 to 69 dB. Still, the company isn't satisfied and is working on a higher speed amplifier, the LM7131 (from $1.55 to $1.85), for release next month.

The basic problem with rail-to-rail amplifiers, says National Application Engineer Bill McDonald, is that there isn't much gain in the amplifier's feedback when the op amp is operating near the rails. This lack of gain causes settling problems, particularly if the ADC

LOOKING AHEAD

Current and future challenges for op-amp designers include achieving lower noise and distortion for high-resolution and high-speed ADCs. However, you won't see a flurry of activity in this area because of these ADCs' lower volumes compared with other ADC types.

For single-supply systems, op-amp designers will have to continue to design innovative circuit structures to improve drive capability, settling time, and distortion at high bandwidths. You will see more single-supply amplifiers with improved ac specifications.

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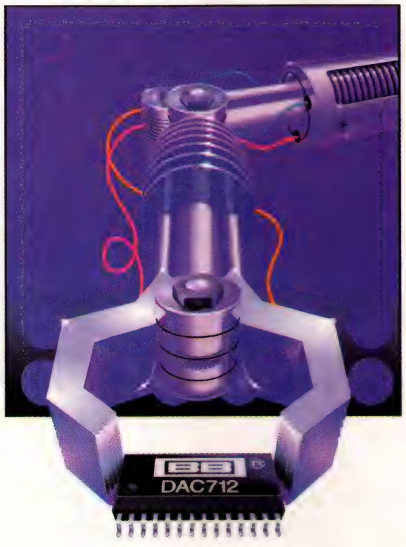

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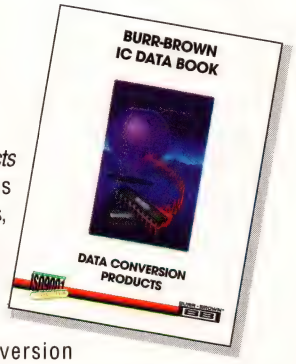

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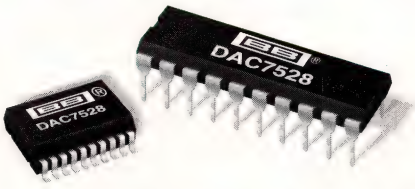

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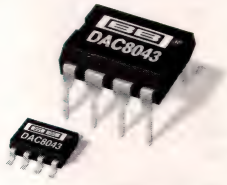

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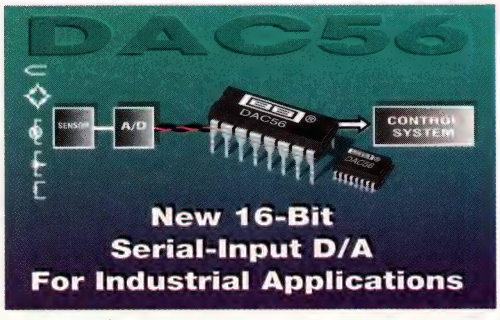

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input kicks back any unusual current or charge spikes. Thus, at peaks of a sine wave, settling becomes more difficult and can potentially lead to increased second-harmonic distortion. The LM7131's design provides adequate gain bandwidth even for signals close to the supply rail. The unity-gain crossover frequency is around 70 MHz.

Performance is not the only reason that lower supply voltages complicate your choice of a drive amplifier. The input-voltage range of new high-speed, single-supply ADCs is not ground-referenced but is centered around some common-mode voltage between ground and the positive supply. For instance, the input-voltage range can be 2V p-p centered around 3V. Thus, if you start with a ground-referenced input signal, you need to either ac-couple or level-shift the input with a single-supply op amp that also has the necessary distortion specifications and drive capability.

Level-shifting is important not only because of changing supply voltages but also because of changing ADC input ranges. Gone are the days of wide input ranges for most ADCs. Many input ranges are now 1 to 2V, which you may need to shift before the ADC input. You can level-shift using an op amp and resistors or using difference amplifiers, such as Analog Devices' AD830 ($2.42) and Linear Technology's LT1187 ($2.85).

You don't necessarily have to drive a 5V ADC with a 5V op amp. As long as you pay attention to the ADC's input and common-mode range, you can use a ±5 or ±15V amplifier. You may need to take steps to protect the ADC. For example, each member of the Burr-Brown's ADS family includes a front-end resistor that provides inherent input-overvoltage protection. However, all ADCs do not offer such protection. For such cases, clamped amplifiers can prevent the amplifier from driving the ADC with an out-of-range signal. Most clamped amplifiers and those with output limits need to recover from saturation quickly to keep the ADC from going into saturation.

Comlinear, Harris, and Analog Devices produce amplifiers with output limits. Harris' 350-MHz HFA1135 (around $3) runs on ±5V supplies and has a maximum saturation recovery time of 1.5 nsec. Analog Devices has also just released two clamped amplifiers, the AD8036 and AD8037 (both $4.12), which feature high-speed and second- harmonic distortion around 72 dB at 20 MHz. Thus, these devices are suitable for 10-bit systems and implement the clamping at the amplifier's input, which the company says pro-

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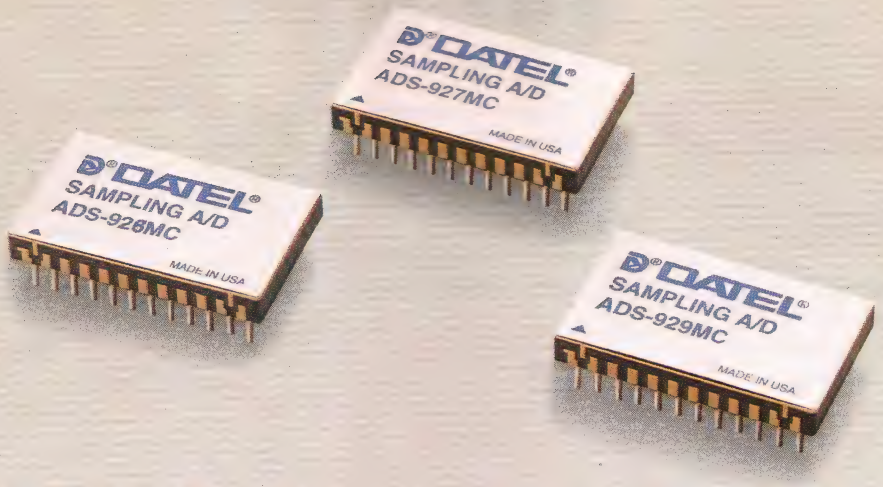

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Focus on ADC inputs

In addition to picking the right amplifier from strictly a performance point of view, a second major factor governing the amplifier choice is the ADC's input structure. Flash converters, with their notoriously nonlinear and high input capacitances, were formerly the most difficult ADCs to drive. Now switched-capacitor input structures are usurping that reputation.

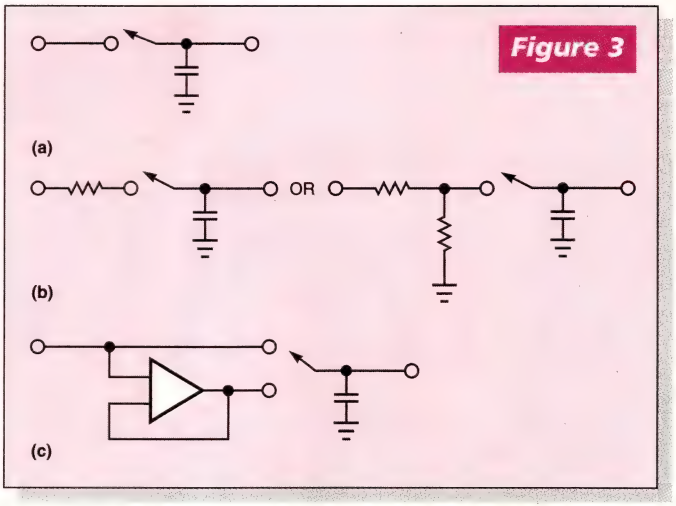
In general, all ADCs fit into one of three groups, depending on whether they have benign, flash, or switched-capacitor inputs.

Benign ADCs have reasonably high and mostly constant input impedances and cause no unusual perturbations at the output of the op amp during sampling intervals. Many of Analog Devices' bipolar ADCs, such as the 1671, 871, 872, 9022, and 9023, fit into this category.

Although flash converters used to routinely require high current at high speed to drive their high input capacitances, manufacturers such as Signal Processing Technology have reduced the problem in new flash converters. Five years ago, a 150-MHz part from the company had a 45-pF input capacitance. Now, newer architectures and processes make possible a 150-MHz ADC with 10-pF capacitance.

Converters with switched-capacitor sampling inputs are the newest genre of ADCs. Many types of ADCs, including almost all CMOS types and high-resolution delta-sigma and audio ADCs, now feature these inputs. An ADC with this switching structure doesn't automatically have high input impedance, and the input impedance can change during the sampling cycle. These inputs also cause transient currents that shock and disturb the op amp's output. The op amp then must settle back to its original buffered or amplified version of the input signal before the next conversion.

Unfortunately, it's virtually impossible to tell from op-amp settling-time specifications what the settling performance will be under these circumstances. Settling time after a transient event at the output is not the same as the settling time a company specifies on op-amp data sheets. Normal settling time refers to how long an amplifier's output takes to settle based on a step change at the amplifier's input. In driving switched-capacitor ADCs, the output is at the desired level, but the ADC perturbs this output. No op amp data sheet directly addresses this type of output settling time.



Switched-capacitor input structures are not all the same. To reduce the transient currents produced by the basic unbuffered-capacitive-sampler structure in (a), some manufacturers have added series resistors, as in the resistive-input sampler (b), and others implement a front-end coarse-charge buffer (c). (Courtesy Jerome Johnston of Crystal Semiconductor)

However, it *is* possible to get some idea of how an amplifier will react to transients by looking at phase-vs-frequency curves. If the phase response rolls off in a smooth linear fashion, the op amp will likely settle fairly effectively after an output glitch. Without a smooth roll-off, especially near the crossover frequency, peaking in the response of the amplifier will occur. Too much peaking implies that the amplifier lacks a well-behaved transient response and will have difficulty driving the ADC's transient load.

You can also take steps to minimize the effects of the output transient. The most important step is to ensure that the amplifier maintains a low output impedance *over all input frequencies of interest*. Op amps with high output impedances can't quickly respond to changes in an ADC's input capacitance or handle the transient currents the ADC kicks back. If the op amp doesn't settle in time for the next conversion, nonlinearities can result.

By looking at single data-sheet numbers, you might assume that most op amps have a fairly low and constant output impedance. However, most data-sheet numbers apply only when the amplifier has sufficient loop gain. Also, output-impedance-vs-frequency curves often stop short of revealing what happens at high frequencies. If the dynamic load placed that the ADC places on the amplifier is beyond the amplifier's unity-gain crossover frequency, the output impedance can be quite high.

Remember that high loop gain is necessary for low output impedance, according to the following equation:

$$R_{OUT} \approx R_O/1+A\beta,$$

where R_O is the open-loop output impedance and $A\beta$ is the loop gain. As you get closer to the unity-gain crossover frequency of the op amp, $A\beta$ decreases, leading to increased output impedance (**Fig 2**).

This impedance requirement then translates directly to a bandwidth requirement. A higher bandwidth op amp has higher loop gain and thus lower output impedance at higher frequencies. According to Harris Semiconductor linear-product-marketing engineer Chris Henningsen, this is one reason to use an 800-MHz amplifier in front of a 20-MHz ADC, which is sampling a 5-MHz video-input signal. The high-bandwidth op amp more effectively swamps out the ADC's kickback signals than does a lower bandwidth amplifier.

According to Linear Technology's Rempfer, op amps with emitter-follower outputs running with lots of current

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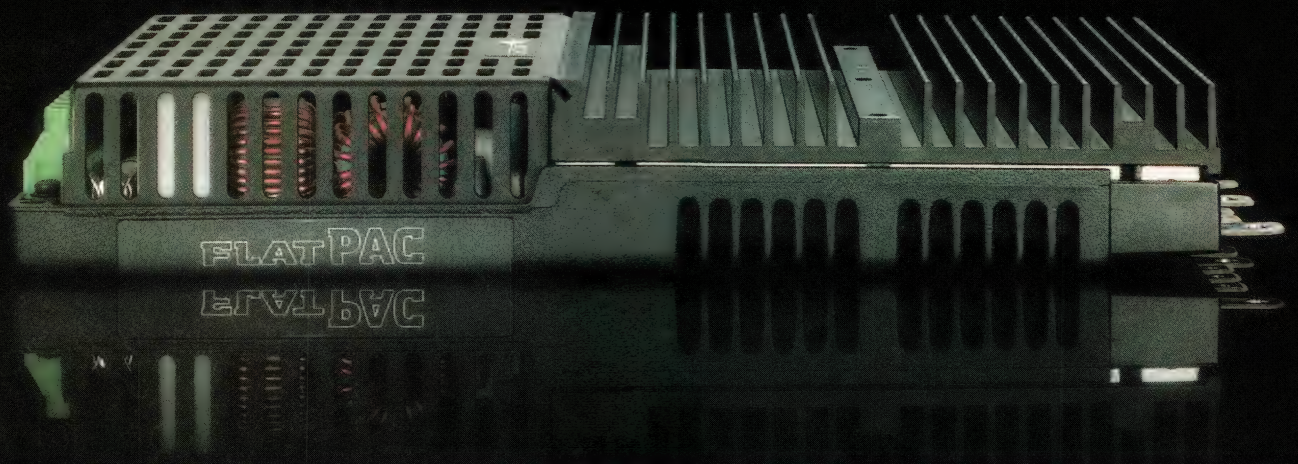

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usually have the necessary low output impedance. One thing to watch out for, however, is amplifiers with inherently higher output impedances, such as those with collectors driving the output—specifically, amplifiers with rail-to-rail outputs.

Inputs have their differences

Manufacturers are also doing their part to minimize the effects of the ADC's transient glitch by modifying the switched-capacitor input. You now find ADCs with the following three types of inputs: (**Fig 3**):

- input directly connected to sampling switch,
- input series resistor before switch,
- coarse-charge buffer.

Burr-Brown's ADS family of pin-compatible 12- and 16-bit ADCs are an example of the input-series-resistor-before-switch structure. The designers put a series resistor on the input so that charge doesn't go straight into the op amp. The ADC designers also reduced the switching current by 10. The result, according to Burr-Brown, is that any amplifier can drive members of the ADS family.

Crystal Semiconductor uses the coarse-charge buffer approach in its CS5101A ADC and all its dc-accurate delta-sigma parts (CS5504 through CS5509). The input switch connects either to a CMOS unity-gain buffer amplifier or to the input signal. The coarse-charge buffer charges the hold capacitor to a signal near the input. When the switch connects to the input, the driving circuit has only to provide charge to compensate for the buffer's offset voltage. The result is that the ADC produces low transient current.

These improvements don't mean you can ignore the amplifier, however. Crystal Semiconductor Applications Engineer Jerome Johnston still fields calls from customers who complain about missing codes, presumably caused by a poor-performing ADC. Johnston says the problem isn't usually the ADC, but a poorly selected amplifier that has difficulty settling properly, particularly around bipolar zero. The company recommends placing an RC network between the op amp and ADC to buffer the dynamic transient current from the ADC. Choose the RC values so that the time constant of the network isn't too long, which would produce averaging and offset errors.

Linear Technology and Maxim Integrated Products also often recommend a 100-pF capacitor to ground between the op amp and ADC to absorb the transient glitch. Adding this capacitor means that the amplifier has to be able to drive this 100-pF load.

In fact, Linear Technology has just introduced a rail-to-rail amplifier, the LT1368 (no prices are available as this article goes to press) that requires and, thus, is happy driving, a 0.1-µF compensation capacitor on the output. When driving an ADC—typically a low-power and low-frequency device such as the LTC1288—this capacitor forms a filter that reduces the amplifier's output impedance and swamps the current spikes from the ADC. In ADC tests with input signals under 100 Hz, the LT1368 shows less than 1 dB of distortion.

Some final words of advice: Beware of what may happen if you run an op amp at other than the tested and specified power-supply voltages; don't scrimp on testing your own op-amp/ADC pair. EDN

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2. Kester, Walt, "Designer's guide to sampling A/D converters," Parts 1 and 2. *EDN*, Sept 3, 1992, pg 135 and Oct 1, 1992, pg 97.

Acknowledgments

Many thanks for useful discussions. Paul Errico, Jay Cormier, and Steve Ruscak of Analog Devices; Jerome Johnston of Crystal Semiconductor; and Willie Rempfer and Bill Gross of Linear Technology.

You can reach Technical Editor Anne Watson Swager at (215) 645-0544.

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VISUAL PROGRAMMING PERVADES DATA-ACQUISITION SOFTWARE DEVELOPMENT

BRIAN KERRIDGE, SENIOR TECHNICAL EDITOR

The first thing you do when devising almost any project or system is to sketch an overview block diagram. Next, you study each block in turn and layer on more and more textual detail until you have a complete description of the design.

Visual programming—also known as graphical, diagrammatic, or iconic programming—for data-acquisition systems works in exactly that fashion. In visual programming, the blocks are preprogrammed software modules that appear as icons on your display. You select and connect icons representing sensor inputs, ADCs, and display outputs in a logical sequence. Some of the icons, such as displays, are standard for any application, but others correspond to hardware specific to your measurement system. Clicking on an icon opens a dialog box containing a range of properties for that icon's function. For an ADC card, you type in properties such as channel number, sample rate, and voltage range. Other icons enable you to insert a wide range of math functions to operate on input signals, such as statistical, algebraic, and frequency-domain operators. Finally, and what gives visual programming its greatest impact, you have icons for building a highly impressive user interface for your system. Sliders, pushbuttons, gauges, meters, and graphs offer you unlimited scope in devising a front panel just to your taste.

Visual programming gets your data-acquisition system up and running in hours or days, instead of the months needed to use traditional coding in Basic or C. MS Windows is the most popular environment, but its interrupt latency can threaten data integrity in high-speed and control-system applications.

National Instruments' LabView visual-programming software, which now runs under MS Windows, is a general-purpose tool with extensive icon libraries for data acquisition, instrument control, data analysis and presentation (Ref 1). Device drivers exist for over 100 programmable IEEE- 488, VXI, and RS-232C instruments, in addition to the company's range of PC plug-in data acquisition, DSP, and signal conditioning hardware.

The overriding benefit of visual programming for data-acquisition systems is the speed with which you can set up a system to take measurements. Traditionally, you could expect to employ the services of a software engineer for a couple of months to code in Basic or C before taking a single measurement. With visual programming, you can reasonably expect to reduce the two months spent coding to two days programming visually. The major gain results from the virtual eclipse of a software programmer to make the system run. Experience shows that scientists, hardware engineers, and system developers can easily exercise visual-programming software in the same way they would string together the hardware itself.

DATA-ACQUISITION SOFTWARE

This feature makes visual programming motivational, fun, and naturally appealing, especially when compared with conventional coding, which is irritating and has little to do with the primary objective of acquiring data.

Additionally, visual programming benefits a wide range of users from the lone technologist to companies developing commercial applications. A technologist's priority is to gather data with minimal sidetracking; commercial developers have an overwhelming desire to reduce time to market.

Visual programming has existed for over a decade. One of the first products, National Instruments' LabView, mainly set out to simplify the programming of rack-and-stack IEEE-488 instrumentation systems. Over that decade, volumes of PCs running MS Windows have outstripped IEEE-488 systems, and, now, the major business for visual programming is operating PC plug-in and standard bus cards.

National Instruments' highly developed LabView remains a leading-market product, although most self-respecting PC-card vendors now offer a competitive product.

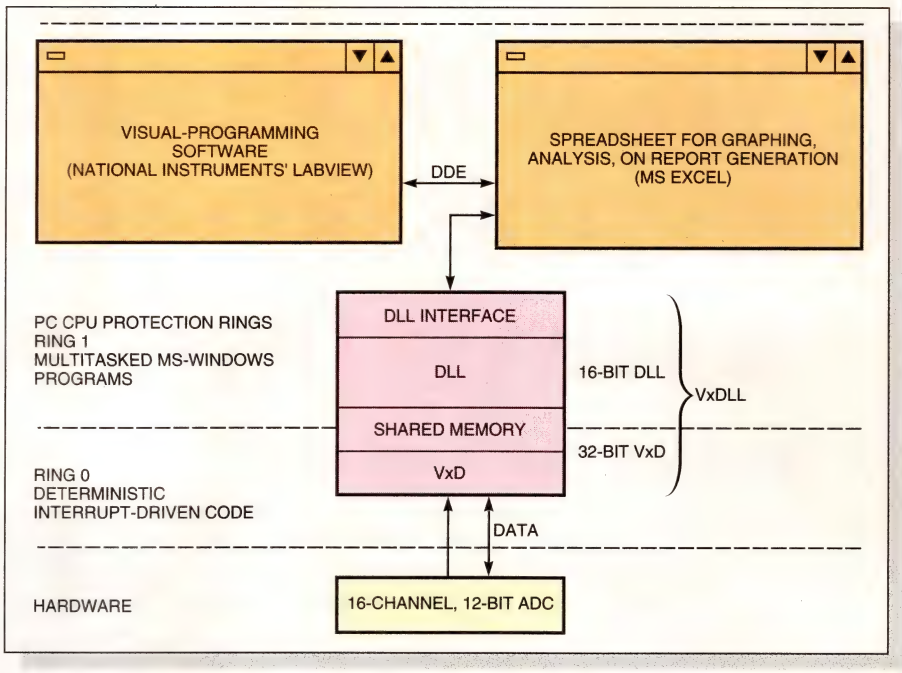

Fig 1— Arcom Control Systems overcame much of MSWindows' interrupt latency by designing virtual DLL SuperDRIVERS (VxDLLs) for users of their hardware data-acquisition products. VxDLLs operate at low-level "Ring 0" in an MS Windows environment and enable I/O interfaces to respond to 10,000 interrupts/sec—sufficient for a wide range of data-acquisition and control applications.

Rival products look alike

Table 1 surveys a selection of visual-programming data-acquisition software products. At first glance, it's not easy to distinguish product offerings. (**Ref 2** reports on a basic bench test of seven of the products listed.) One basic difference is that some products, such as LabView, are stand-alone programs, and later products, such as Keithley's Visual DAS, are adaptations of MS Visual Basic. Also, price does little to distinguish products, and $995 is a popular number. Prices shown are for software to develop applications, although some vendors offer lower cost run time-only versions. Implementations using MS Visual Basic are lower cost, although you need to add around $199 for Visual Basic.

One product-to-product variation worth investigating is the range of software device drivers that each vendor supplies. Some vendors provide drivers for only their own range of plug-ins, which effectively obliges you to use their data-acquisition hardware. In contrast, an increasing number of third-party hardware suppliers offers MS Visual Basic and Visual C++ drivers that provide more of an open-system environment to developers using these programs.

Another important factor is the effectiveness of the driver. There's no simple to way to compare drivers, and you need to thoroughly evaluate performance before committing to a visual-programming or hardware product.

Although visual programming largely negates the need to be a software programmer, C designers need not fear for job security yet. First, writing software drivers for I/O hardware remains a prime requirement. Drivers involve significant coding, and writing your own can easily consume a man-year of effort. Second, although running data-acquisition systems under MS Windows is very appealing, Windows introduces a heavy cost and physical-size overhead and imprecise timing to the system.

The cost overhead results from the need for a posh PC to run MS Windows and a visual-programming environment. To run Hewlett-Packard's HP-VEE, for example, the company recommends a 33-MHz 80486 PC with a 1024×768-pixel SVGA display, a 16-Mbyte RAM, and 15 Mbytes of hard-disk space. In comparison, a C program would certainly run on an embedded 20-MHz 80386 processor card with less

LOOKING AHEAD

Visual programming will continue to make inroads into the traditionally coded data-acquisition software territory. The installed base of MS Windows environments will ensure its continued popularity. When MS Windows 4.0 (Chicago) arrives, true multitasking ability promises to expand the scope of data-acquisition systems and should address some existing Windows interrupt-latency concerns. Software speed problems will also diminish as 66-MHz, and beyond, PCs become the norm.

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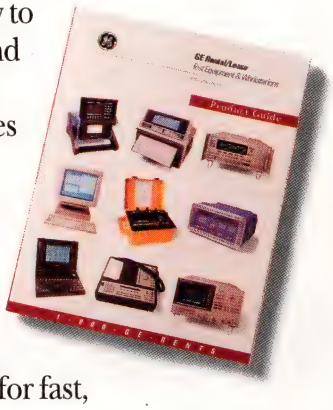

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Relying on an MS Windows environment to control system timing is far from ideal for some data-acquisition setups. In practice, MS Windows relies on a PC's 55-msec interrupt latency, which is insufficiently deterministic for high-speed data-acquisition or control systems. (Interrupt latency is a measure of the time between an interrupt's asserting that data is available and the point when the CPU reads the data.) MS Windows was never intended to drive speed-conscious hardware and can't hope to compete with dedicated code running under real-time operating systems.

A further justification for retaining some traditionally programmed C-coded data-acquisition software involves safety-critical control-system applications. Without a great deal of beta-site testing, you can't be sure that either MS Windows or the visual-programming environment won't decide to display an obscure dialog box that halts a process at a critical point. With your own C code, you are still required to beta-test, but, overall, there are fewer unknowns in your own control software.

Programming know-how helps

Although visual programming claims that the user does not need not traditional programming skills, some programming experience can benefit your work. Also, some familiarity with MS Windows features such as Dynamic Data Exchange (DDE) and Dynamic Link Library (DLL) is important. Briefly, DDE is a standard MS Windows message-handling system for importing or exporting data between applications. A DLL is a Windows program providing functions that other Windows programs can use when driving I/O hardware, for example.

According to Stephen Salmon, software-design engineer with Arcom Control Systems, "There's no doubt visual programming enables most technologists to swiftly make a system produce results, although users' initial attempts may produce inefficient and inelegant solutions."

Comparing learning curves using different approaches, Salmon decided that, after two years of coding in C, he was competent enough to design software for data-acquisition systems. Moving on to LabView, he found that he could produce an equivalent system after a matter of days. (Because Visual Basic offers developers more program visibility, using Visual Basic takes a few days longer.)

Salmon advises visual-programming users to think carefully through their early applications and attempt to simplify their designs. He reports that new users typically employ several individual channels from input to display rather than introducing multiplexing. Unnecessarily duplicating sequential- and repetitive-event icons, instead of using for and while loops is another common overcomplication. Littering the display with icons rapidly eats memory that is needed to run a system and can limit operating speed because the program has to interpret the superfluous icons in the run mode.

Salmon also draws attention to the effect of Windows' inherent interrupt latency on operating speed. In many cases, a system's read rate is sufficiently slow that interrupt latency is not significant, as in a temperature-logging system that takes readings every few minutes. But, for high-speed data-acquisition or -control systems, it's important to know precisely when measurements occur, as in real-time logging.

To minimize the effects of interrupt latency, Arcom uses a special form of virtual extended-DLL driver (VxDLL) with its range of hardware, called a "SuperDriver." VxDLLs operate at low-level "Ring 0" in an MS Windows environment, predictably trapping interrupts and enabling I/O interfacing independent of the host program (**Fig 1**). Any Windows-based program that supports DLL or DDE, such as Visual Basic, Visual C++, or LabView, can call Arcom's SuperDriver code.

Arcom has compared the interrupt-

TABLE 1—REPRESENTATIVE VISUAL-PROGRAMMING DATA-ACQUISITION SOFTWARE

Vendor	Product	Computer type				Requires MS Visual Basic	Price
		Mac	PC		W/S		
			W 3.1	NT			
Analogic Circle No. 341	Snap-Master		X				$995
Capital Equipment Circle No. 343	Testpoint		X				$995
Data Translation Circle No. 344	DT VEE		X				$1995
	VB-EZ		X			X	$195
G-W Instruments Circle No. 345	Superscope II	X					$1490
Hewlett-Packard Circle No. 346	VEE		X	X	X		$1995
Intelligent Instrumentation Circle No. 347	Visual Designer		X				$995
IOTech Circle No. 348	VisuaLab		X			X	$395
Keithley Instruments Circle No. 349	VisualDAS		X			X	$99
Laboratory Technologies Circle No. 350	Labtech Notebook		X				$995
Microstar Laboratories Circle No. 351	DASYLab		X				$9
	DAPwindows		X				$295
National Instruments Circle No. 352	LabView	X	X	X	X		$995
Omega Circle No. 353	Centrel	X					$198
Strawberry Tree Circle No. 355	Workbench PC		X				$995

Prices shown for base application-development software. Additional advanced-development tool kits and extra device-driver libraries can double base price. Some vendors offer run-only versions under $500.

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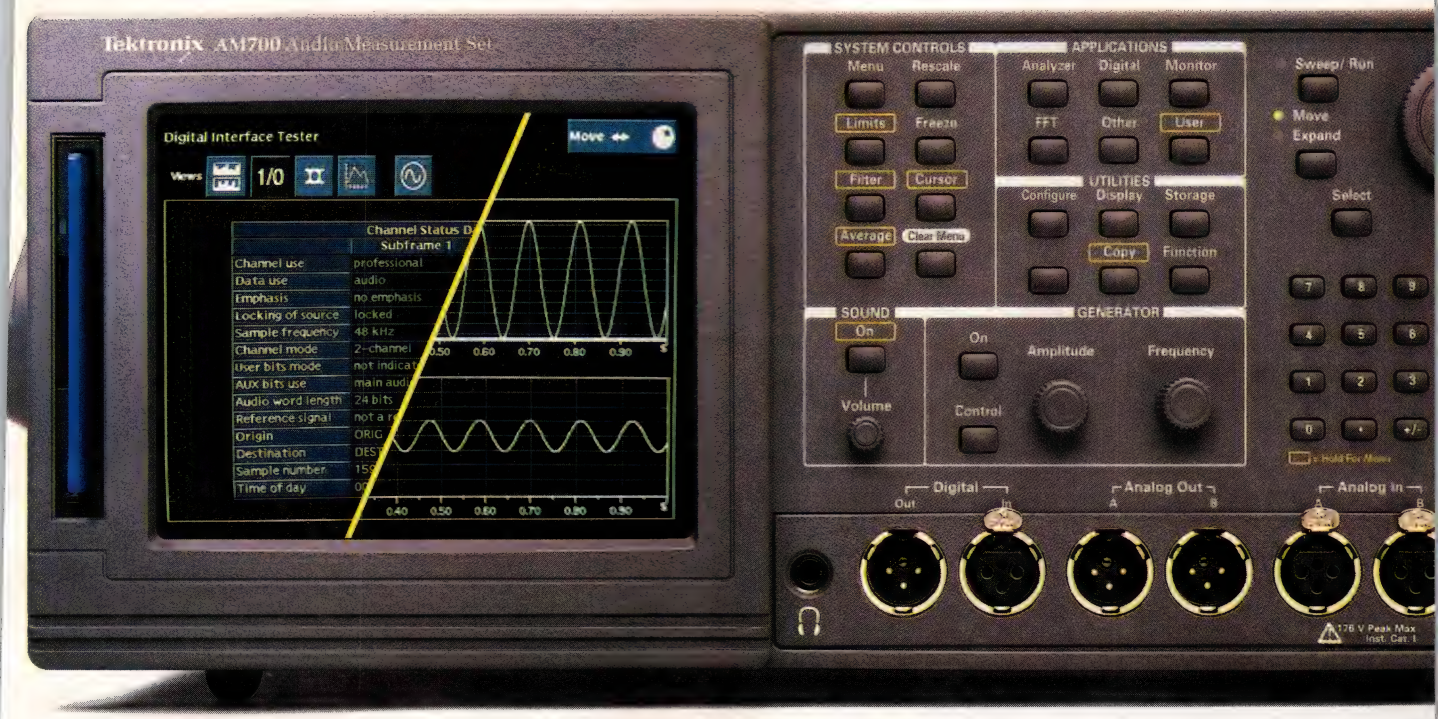

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latency performance of its SuperDrivers with other MS-DOS and the Windows VxD drivers using a 40-MHz 80386DX CPU. Results show a range of latencies for each driver: MS-DOS mouse device driver running under Windows—100 to 400 µsec, Windows terminal emulator—40 to 65 µsec, and Arcom's SuperDriver—25 to 50 µsec.

Microstar Laboratories use a different approach to minimizing interrupt-latency effects. The company's PC plug-in data-acquisition boards include an on board processor, memory, and a real-time operating system called DAPL. This on board intelligence handles the time-critical aspects of an application and frees your data-acquisition hardware from delays and resource demands imposed by Windows. Running under the company's DASYLab visual-programming software, the processor typically achieves a task latency of <500 µsec. EDN

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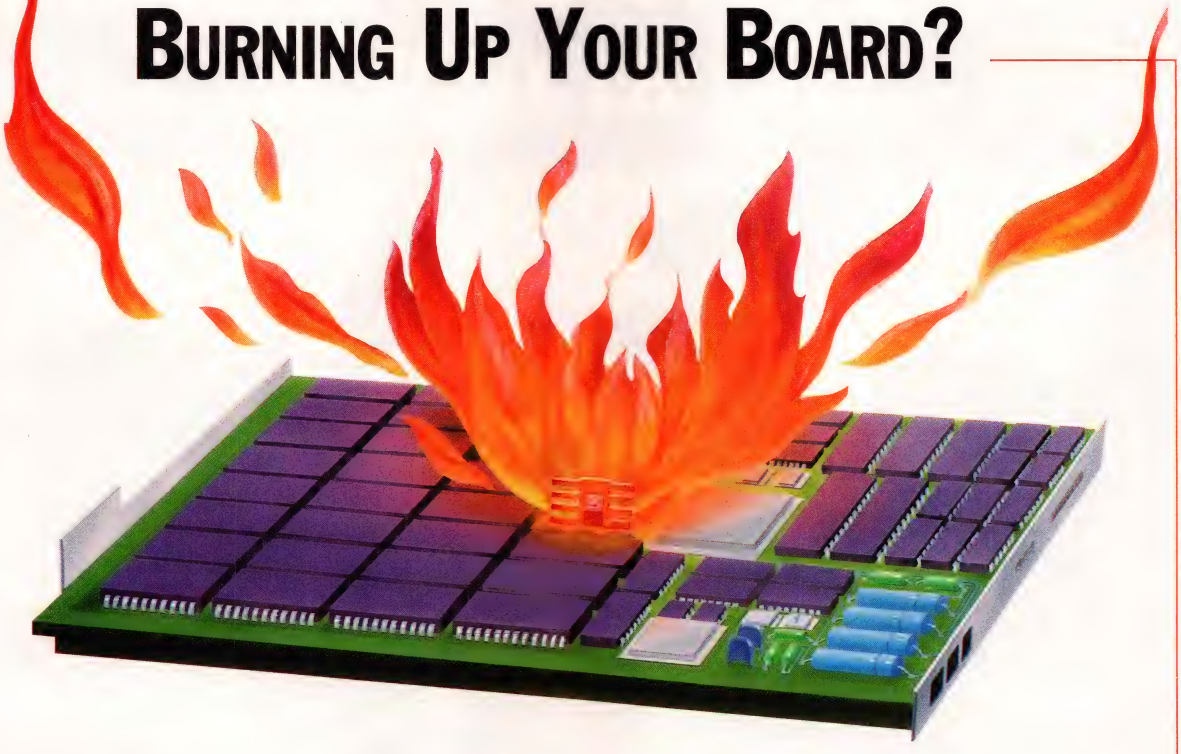

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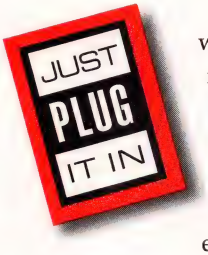

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CIRCLE NO. 39

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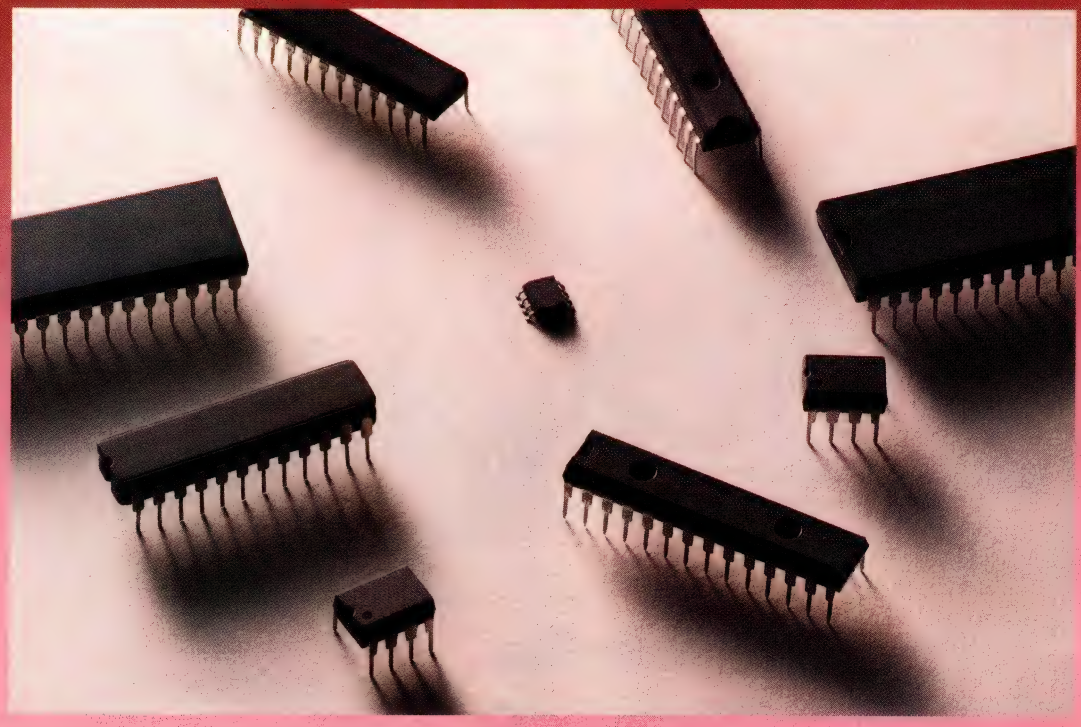

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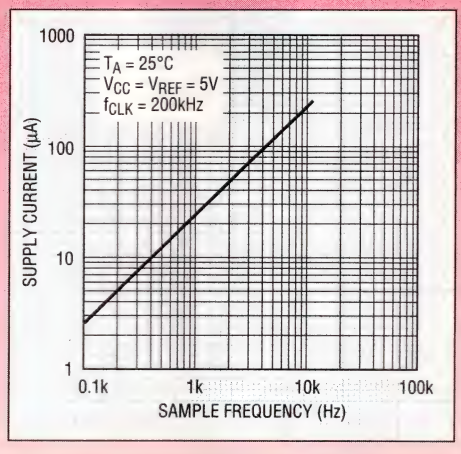

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CIRCLE NO. 79

LINEAR TECHNOLOGY

DESIGN NOTES

Fast Regulator Paces High Performance Processors

Design Note 87

Mitchell Lee and Craig Varga

New high performance microprocessors require a fresh look at power supply transient response. Pentium™ processors, for example, have current demands that go from a low idle mode of 200mA to a full load current of 4A in 20ns. A transition of the same magnitude occurs as the processor reenters its power saving mode. In addition, the overall supply tolerances have been narrowed significantly from the traditional ±5% for 5V supplies and include transient conditions. When all possible DC error terms are accounted for, the transient response of the power supply when subject to the load step mentioned above must be within ±46mV!

To address this problem Linear Technology has developed the LT1585 linear regulator. It features 1% initial accuracy, excellent temperature drift and load regulation, and virtually perfect line regulation. Complementing superb DC characteristics, the LT1585 exhibits extremely fast response to transients. The regulator is offered as an adjustable regulator requiring two resistors to set the operating point, as well as fixed versions which have been trimmed and optimized for 3.3V, 3.38V, 3.45V, and 3.6V outputs. Fixed versions are fully specified for worst-case DC error bounds; in adjustable designs the effects of the external voltage-setting resistors must be taken into account.

Transient response is affected by more than the regulator itself. Stray inductances in the layout and bypass capacitors, as well as capacitor ESR dominate the response during the first 400ns of transient. Figure 1 shows a bypassing scheme developed to meet all of the requirements for the Intel P54C-VR microprocessor. Multiple capacitors are required to reduce the total ESR and ESL, which affect the transient response.

Input capacitors C1 and C2 function primarily to decouple load transients from the 5V logic supply. The values used here are optimized for a typical 5V desktop computer "silver box" power supply input. C5 to C10 provide bulk capacitance at low ESR and ESL, and C11 to C20 keep the ESR and ESL low at high (>100kHz) frequencies. C4 is a damper and it minimizes ringing during settling.

A good place to locate the surface mount decoupling components is in the center of the Pentium socket cavity on the top side of the circuit board. Consider using concentric rings of power and ground plane on the top layer of the board within the socket center for bussing the

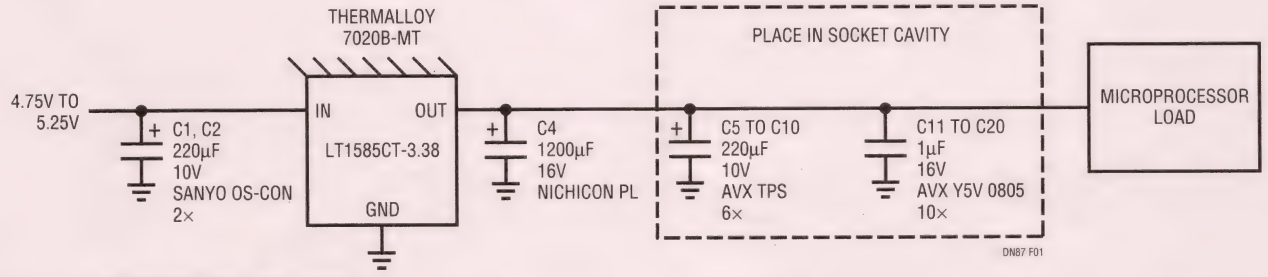

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Figure 1. Recommended Bypassing Scheme for Correct Transient Response

capacitors together. Tie the main power and ground planes to these cavity planes with a minimum of two vias per capacitor. This will minimize parasitic inductance. The regulator and damper capacitor should be located close to (<1") the microprocessor socket to minimize circuit trace inductance.

Verifying the regulator and microprocessor layout can be accomplished with a controlled load such as the Power Validator™ manufactured by Intel. This device plugs directly into the microprocessor socket and simulates worst-case load transients conditions.

An oscilloscope photograph of the LT1585's response to a worst-case 200mA to 4A load step is shown in Figure 2. Trace C is the load current step, which is essentially flat at 4A with a 20ns rise time. Trace A is the output settling response at 20mV per division. Cursor trace B marks

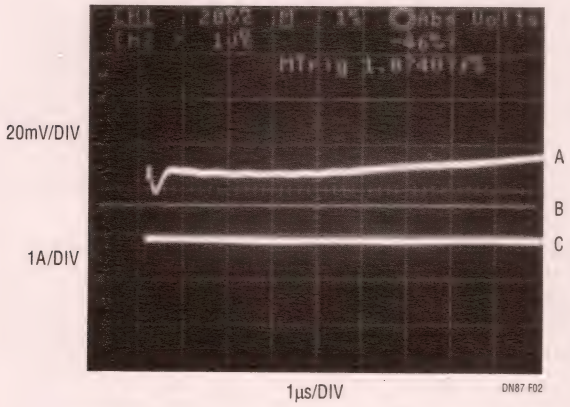

Figure 2. Transient Response at Onset of 4A Load Current Step

–46mV relative to the initial output voltage. At the onset of load current, the microprocessor socket voltage dips to –38mV as a result of inductive effects in the board and capacitors, and the ESR of the capacitors. The inductive effects persist for approximately 400ns. For the next 3µs the output droops as load current drains the bypass capacitors. The trend then reverses as the LT1585 catches up with the load demand, and the output settles after approximately 50µs.

Running 4A with a 1.7V drop, the regulator dissipates 6.8W. The heat sink shown in Figure 1, with 100ft/min air flow is adequate for worst-case operating conditions.

The adjustable version of the LT1585 makes it relatively easy to accommodate multiple mircoprocessor power supply voltage specifications (see Figure 3). To retain the tight tolerance of the LT1585 internal reference, 0.5% adjustment resistors are recommended. R1 is sized to carry approximately 10mA idling current (≤124Ω), and R2 is calculated from:

$$R2 = \frac{V_O - V_{REF}}{\frac{V_{REF}}{R1} + I_{ADJ}}$$

where:

I_{ADJ} = 60µA and V_{REF} = 1.250V

Figure 3 shows the connections for R1 and R2. Note that C5 to C10 are reduced in value from Figure 1 without compromising the transient response. The addition of C3 makes this possible and also eliminates the need for C4.

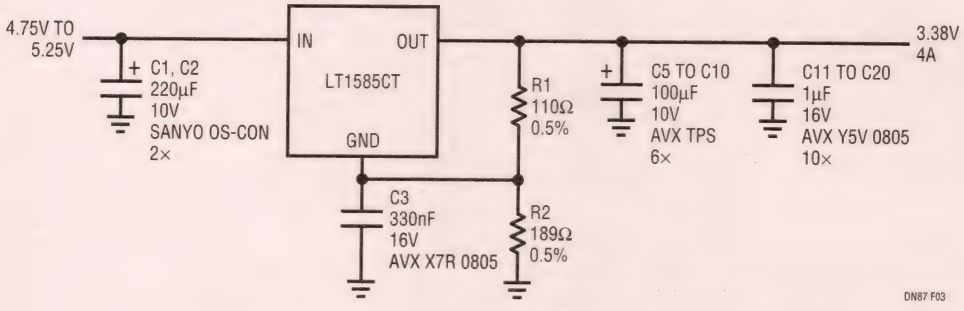

Figure 3. Recommended Adjustable Circuit

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EDITED BY CHARLES H SMALL & ANNE WATSON SWAGER

Spice does digital filters

RICHARD J FAEHNRICH, BIO-IMAGING RESEARCH, LINCOLNSHIRE, IL

BBS

You can use Spice to simulate digital or discrete time filters as well as analog or continuous time filters. Just as you would use integrator blocks to simulate the 1/s terms for an analog filter, you can use Spice's transmission-line component to simulate the ideal z^{-1} delay elements of digital filters.

Fig 1 shows the block diagram and basic third-order transfer function that describe a digital filter. Simulating this canonical or type II direct form can be insightful because you typically realize IIR digital filters from this form. The basic structure and transfer function are identical to that of an analog filter except that z^{-1} terms replace the analog filter's 1/s terms.

Fig 2 shows a Spice circuit for an ideal delay block using a transmission line. The transmission line statement (T1, T2, and T3 in **Listing 1**) requires you to specify the propagation delay time (TD) or, alternatively, the frequency and wavelength. For this application, the delay time is far more useful because it represents the sampling period of the digital filter. The statement also requires a characteristic impedance, Z0. The value isn't critical as long as you terminate the line with a resistor R1 of value equal to Z0.

To simulate the frequency response of a third-order digital filter, you first typically obtain the filter coefficients by applying the bilinear transform to the analog prototype. The bilinear transform substitutes $s=(2/T)\times(1-z^{-1})/1+z^{-1})$ into the analog transfer function. Because the bilinear transform distorts the pole and zero locations of the analog filter, you must prewarp the frequencies before applying the transform to obtain the desired response.

The transfer function for a third-order Butterworth digital filter with a 1-kHz cutoff frequency and 10 kHz sampling frequency is

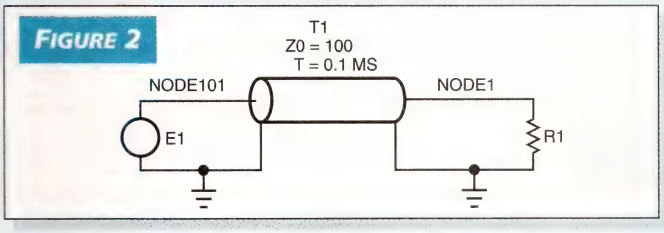
$$H(z)=\frac{0.0181+0.0543z^{-1}+0.0543z^{-2}+0.0181z^{-3}}{1-1.760z^{-1}+1.1829z^{-2}+0.2781z^{-3}}.$$

Listing 1 is the corresponding Spice netlist, and **Fig 3** shows the simulation result. The response resembles a lowpass filter from dc to the Nyquist frequency of 5 kHz. Note the periodic nature of digital filters: The response repeats itself at a frequency interval equal to the 10-kHz sampling frequency. Spice helps you verify that the prewarped frequencies and the bilinear transform produce the required attenuation in the pass and stop bands.

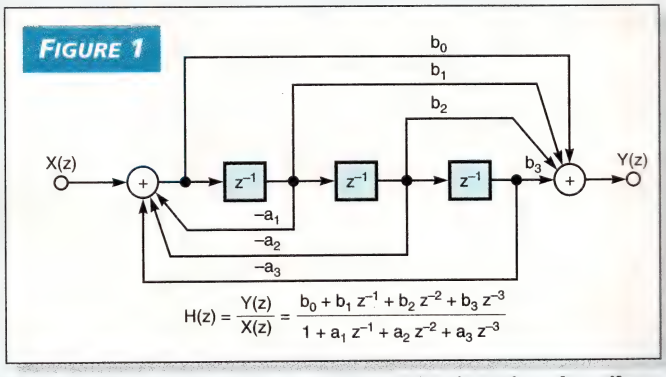
You can also simulate an FIR filter with a similar structure to **Fig 1**, the difference being that an FIR filter's transfer function contains no poles and, thus, the denominator of the

LISTING 1

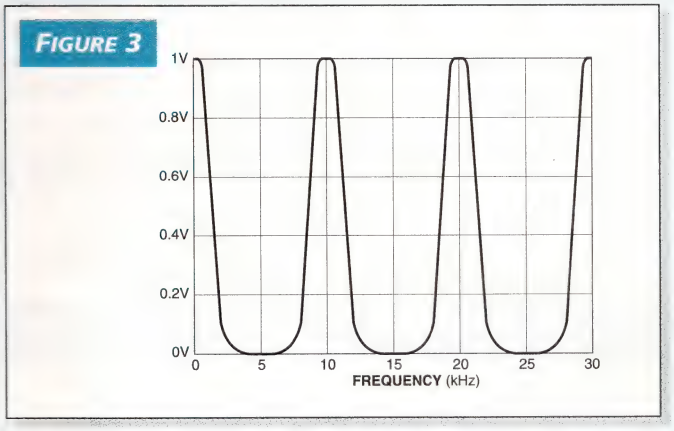
```
ZTF3.CIR - 3RD-ORDER IIR DIGITAL FILTER
* BUTTERWORTH, LOW-PASS, FC=1000HZ, TS=0.1MS
*
VS      10      0       AC      1       DC      1
RS      10      0       1E9
*
* TRANSFER FUNCTION, 3RD-ORDER
* FEEDFORWARD AND FEEDBACK - NUMERATOR AND DENOMINATOR COEFFICIENTS
EY    20 0 POLY(4) (11,0) (1,0) (2,0) (3,0) 0 0.0181  0.0543 0.0543  0.0181
EX    11 0 POLY(4) (10,0) (0,1) (0,2) (0,3) 0 1.0000 -1.7600 1.1829 -0.2781
*
R11     11      0       1E9
R20     20      0       1E9
* DELAY 1
E1      101 0   11 0    1
T1      101 0   1 0     Z0=100 TD=0.1MS
R1      1       0       100
* DELAY 2
E2      102 0   1 0     1
T2      102 0   2 0     Z0=100 TD=0.1MS
R2      2       0       100
* DELAY 3
E3      103 0   2 0     1
T3      103 0   3 0     Z0=100 TD=0.1MS
R3      3       0       100
*
.AC LIN 200 1 10000
.TRAN  0.1MS 3MS 0 0.05MS UIC
.PROBE
.END
```



Spice's transmission-line element serves as the delay or z^{-1} term of a digital filter.



This familiar block diagram and transfer function describe a basic third-order digital filter.



This frequency-response plot of a third-order digital filter resembles a lowpass filter from dc to the Nyquist frequency of 5 kHz. This plot helps you verify that the prewarped frequencies and the bilinear transform produce the required attenuation in the pass and stop bands.

transfer function is equal to 1. However, simulating FIR filters may not be practical because they can have several to over one hundred coefficients. Because each coefficient requires a delay line, one FIR filter may require a large Spice file implying long simulation times.

To simulate and analyze the transient response of a digital filter, you must apply the digital filter to a continuous signal and then sample the continuous output of the filter to obtain the discrete-time results. Theoretically this is possible because a system with ideal delay blocks operates equally well with continuous or discrete input signals. Thus, to simulate the time response of a digital filter, you first perform the standard transient analysis with a continuous-time input and then print the output data only at the sampling period intervals. The print interval, 0.1 msec, of the .TRAN statement performs the "sampling." Some versions of Spice automatically set the maximum time step of the transient analysis to one-half msec times the smallest transmission line delay. For this filter, the .TRAN statement explicitly sets the maximum time step to this value, which is 0.05 msec.

Spice mimics an input step using the 1V dc voltage sourc (VS) and the .TRAN statement. The presence of the UIC para meter in the .TRAN statement directs Spice not to compute the dc-bias solution. Instead, the UIC parameter uses the value in the .IC statement as the initial transient condition Because the file doesn't contain an .IC statement and thus doesn't specify any initial conditions, the initial voltage at VS is 0V. Then, at the first time step, VS assumes its dc value of 1V.

You should be aware of the limitations of using Spice to analyze discrete time structures. First, transmission lines consume large amounts of memory during transient analysis. Second, transmission lines with short delay times compared with the total simulation interval can result in long simulation times. (DI #1585) EDN

To Vote For This Design, Circle No. 375

PC acts as RS-232C protocol analyzer

J S HOLMES, BOEHRINGER MANNHEIM, INDIANAPOLIS, IN

BBS

The circuit in **Fig 1** is an inexpensive and easy-to-build PC-based alternative to a dedicated protocol analyzer. The circuit taps into an RS-232C line between J_1 and J_2, and IC_1's charge pump converts the RS-232C signals to CMOS levels. Many different types of RS-232C charge pumps work well in this circuit. One of the drivers in IC_1 then converts the mixed signal back to RS-232C levels and transmits the data to the PC out of J_3.

The PC must be running a monitor program to use this data. For applications in which the unit under test transmits and receives ASCII data, a commercial terminal emulator program, such as Procomm or Crosstalk, works well. If, however, the data on the signal line is binary, then **Listing 1**'s QuickBasic program can make the data legible.

The program assumes a data rate of 9600 baud. You must make sure that the monitor baud rate matches the baud rate of the unit under test. The most efficient realization of this program involves putting the communication parameters in a file and reading it in at the beginning of execution. The program then goes into an infinite loop. The loop checks to see if there are any characters in the serial port, checks to see if the escape key is pressed, then repeats. In the event that a character comes into the serial port, it is displayed in ASCII and as a decimal equivalent. If you implement this program in a system that communicates with large numbers of characters, you can send the results to a file instead of to the screen. This will allow you to review the results of the communication attempt in a text editor. (DI #1588) EDN

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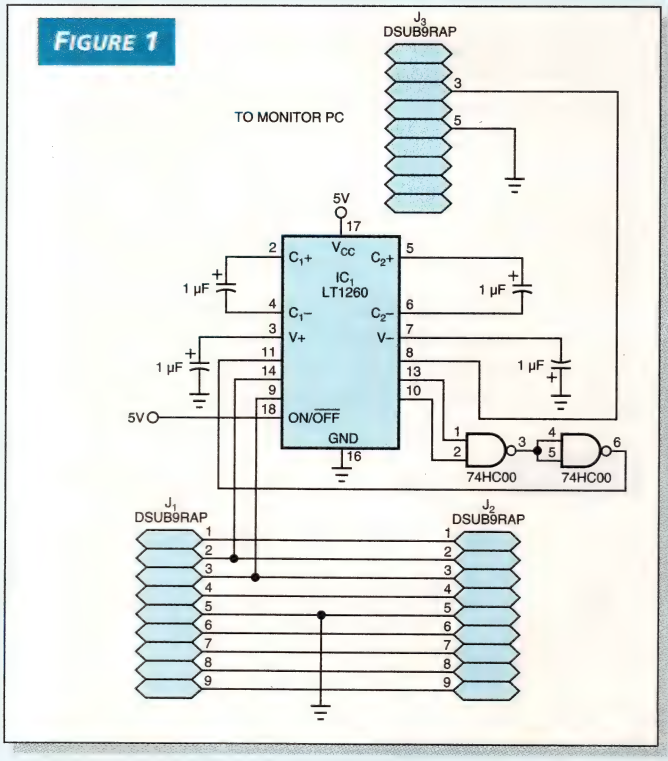
LISTING 1—QUICKBASIC COMMUNICATIONS MONITOR

```
OPEN "COM1:9600,N,8,1,CD,CS,DS,OP,RS" FOR RANDOM AS #99 'Set up 9600 BAUD.
WHILE(1<>0)
      WHILE (LOC(99)=0)
            IF INKEY$=CHR$(27) THEN
                  CLOSE
                  END
                  END IF
            WEND
      TMP$=INPUT$(1,99)
      PRINT "ASCII="; TMP$; " BINARY=";ASC(TMP$)
      WEND
CLOSE
END
```

FIGURE 1



This inexpensive and easy-to-build PC-based alternative to a dedicated protocol analyzer taps into the RS-232C line between J_1 and J_2.

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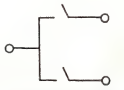

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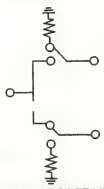
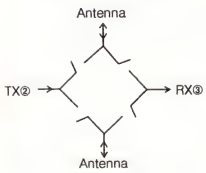


SPDT ABSORPTIVE



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CIRCLE NO. 84

Maximum voltage sorter uses analog multiplexers

ALAN L GILES, TAO SYSTEMS, HAMPTON, VA

The voltage-sorting circuit in **Fig 1** continuously finds the maximum of eight input voltages and the corresponding binary address with the aid of two analog multiplexers, IC_1 and IC_2. The circuit compares each input sequentially with the current maximum voltage and updates the maximum voltage and address when it finds a new maximum. IC_2 and IC_3 act as storage elements. IC_4 ensures that latching can't occur at the beginning or the end of a given address, thereby preventing an incorrect address from being latched at an address transition. The sorter can also find the minimum of its input if you swap the CMP01 comparator's input.

The analog multiplexers, which typically have combined switching and settling times of 0.5 to 1.5 μsec, determine the minimum sorting time of this circuit. Overall sorting time is limited to about 1 μsec multiplied by the number of inputs. Given this constraint, you need to determine the desired overall sorting time and set the clock frequency accordingly. If V_{MAX} is used elsewhere, you should buffer it to avoid a voltage drop across the analog multiplexer's on resistance.

You can expand this eight-input sorter to 16 inputs without increasing the chip count by simply using two 16:1 analog multiplexers instead of two 8:1 multiplexers. This circuit already includes the next counter bit and D flip-flop required for the fourth address bit. You can further double the number of inputs to 32 by using three chips to form two 32:1 analog multiplexers. (DI #1586) EDN

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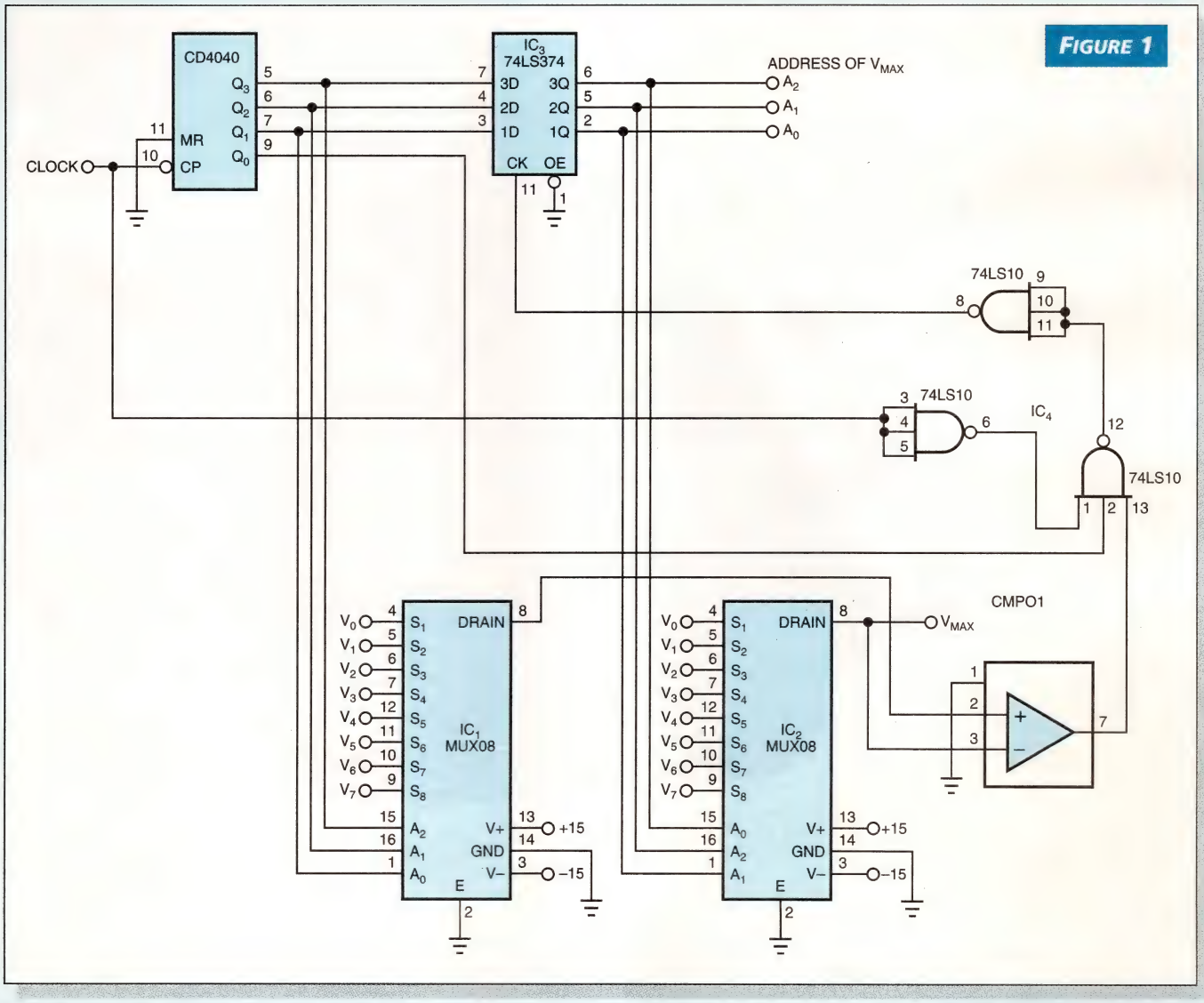

This voltage sorter uses two analog multiplexers to continuously search for the maximum of eight input voltages.

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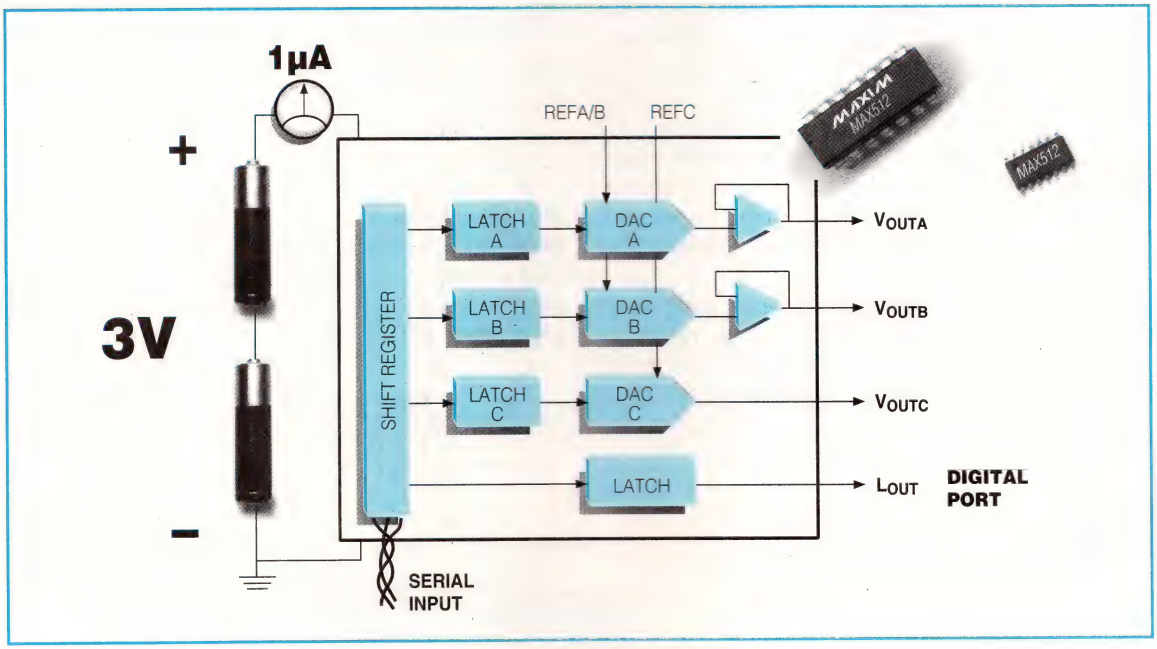

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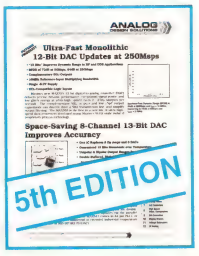

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Frequency comparer produces binary results

JAY KIRSCHENBAUM, COLUMBIA UNIVERSITY, NEW YORK, NY

Instead of resorting to full-blown frequency counters, the simple circuit in **Fig 1** uses four ICs to rapidly compare the frequency of two pulse trains. The circuit produces a binary 0 if f_1 is greater than f_2 and a binary 1 if f_1 is less than f_2. The circuit exploits the fact that inevitably two consecutive leading edges of the higher frequency pulse train will follow each other in time without an intervening leading edge from the other pulse train. The circuit uses two pairs of flip-flops, IC_2 and IC_3, as 2-bit binary counters. A dual monostable multivibrator, IC_1, marks the leading edges of the input pulses by producing spikes of approximately 100 nsec in duration. The circuit couples each stream of spikes to the clock input of one counter and to the reset input of the other.

When one counter's clock receives two consecutive spikes without the arrival of an intervening reset pulse, the high-order bit of that counter goes high. Then, a latch formed by two NOR gates of IC_4 sets or resets depending on which of the two pulse trains has the higher frequency. If f_1 is greater than f_2, the latch resets to 0; if f_1 is less than f_2, the latch sets to 1. The latch holds it state until there is a change in the relative magnitudes of the two frequencies.

For frequencies f_1 and f_2, the maximum response time of the circuit is given by the following

$$T_{MAX} = \frac{1}{f_1} \times \frac{f_2}{\Delta f}, f_2 > f_1.$$

At 1 kHz and for f_1 and f_2 within 1% of each other, the circuit responds within 100 msec. One important note: The circuit is designed to handle asynchronous pulse trains, and it won't work if f_1 and f_2 are synchronous integral multiples of each other. (DI #1587) EDN

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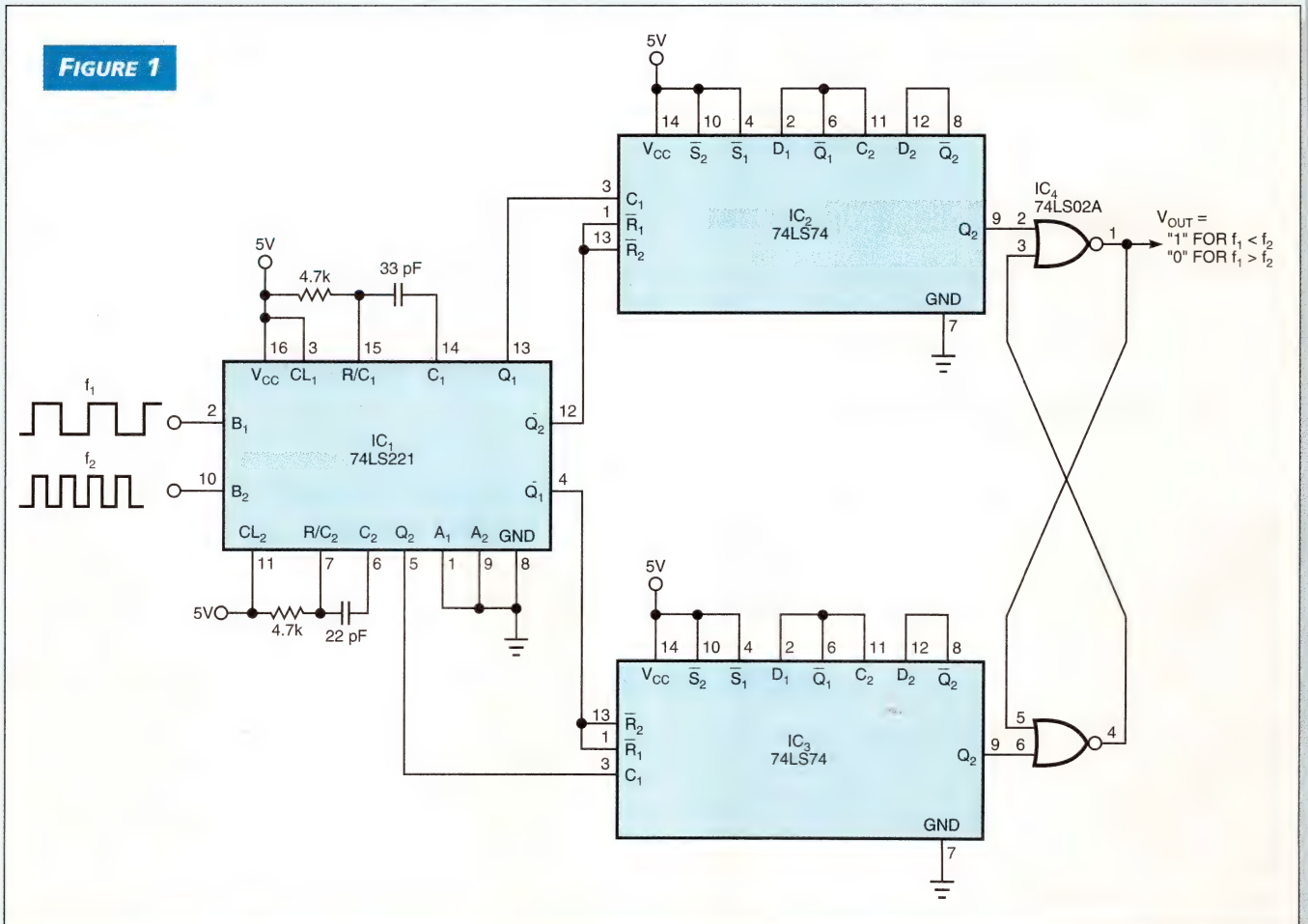
FIGURE 1



If f_1 is greater than f_2, the output of this frequency comparer is a 0; if f_1 is less than f_2, the output is a 1.

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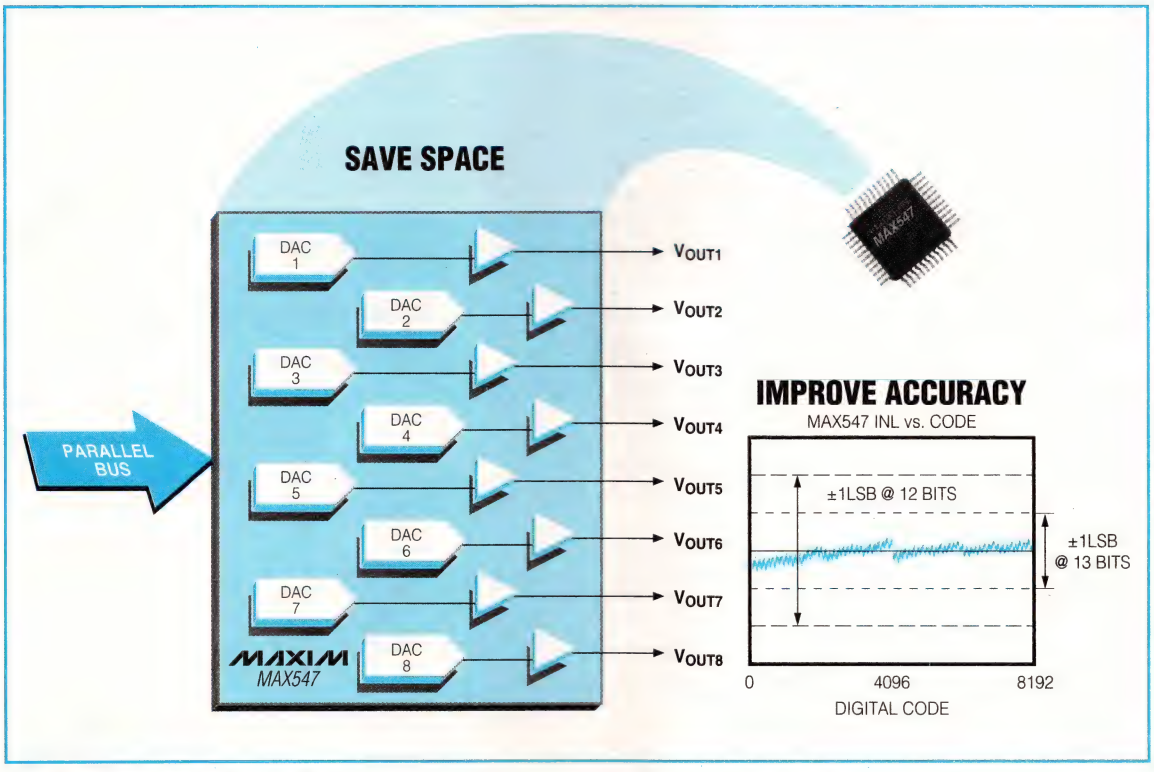

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CIRCLE NO. 81

Power amplifier has transient rail-to-rail swing

YISHAY NETZER, YUVALIM, ISRAEL

Fig 1a's conventional common-drain MOSFET-based power op amp, with a simple and stable configuration, has a dynamic response identical to that of IC_1. However, as a power amplifier, it exhibits a limited-output voltage swing that is typically less than either supply by 6V. This limitation results from the combination of the turn-on voltage of the MOSFET transistors and the limited voltage swing of the monolithic op amp. Usually this deficiency is overcome by an auxiliary pair of higher voltage power supplies for the monolithic op amp. Alternatively, other suggested configurations combine an op amp with a complementary common-source power stage. However, these configurations are inherently unstable and difficult to compensate because of the added wideband gain of the output stage.

In reality, a large voltage swing is necessary only in transient situations and not in the steady state. This is typical of loudspeaker drivers as well as servo-motor drivers. The modified power op amp in **Fig 1b** attains transient rail-to-rail voltage swing by adding just a few passive components to **Fig 1a**'s design. The bootstrapping mechanism implemented by clamping network R_1, C_1, D_1, and D_2 for the positive power supply and by R_1, C_2, D_3, and D_4 for the negative power supply automatically increases the op amp's supply voltage when necessary. R_1 limits the boost amount and protects the output voltage from destroying D_1 and D_4. Along with the supply current of the op amp, C_1 and C_2 determine the cut-on frequency above which the output-voltage-swing range starts to increase. The range is typically 300 Hz for the values in the figure. (DI #1589) EDN

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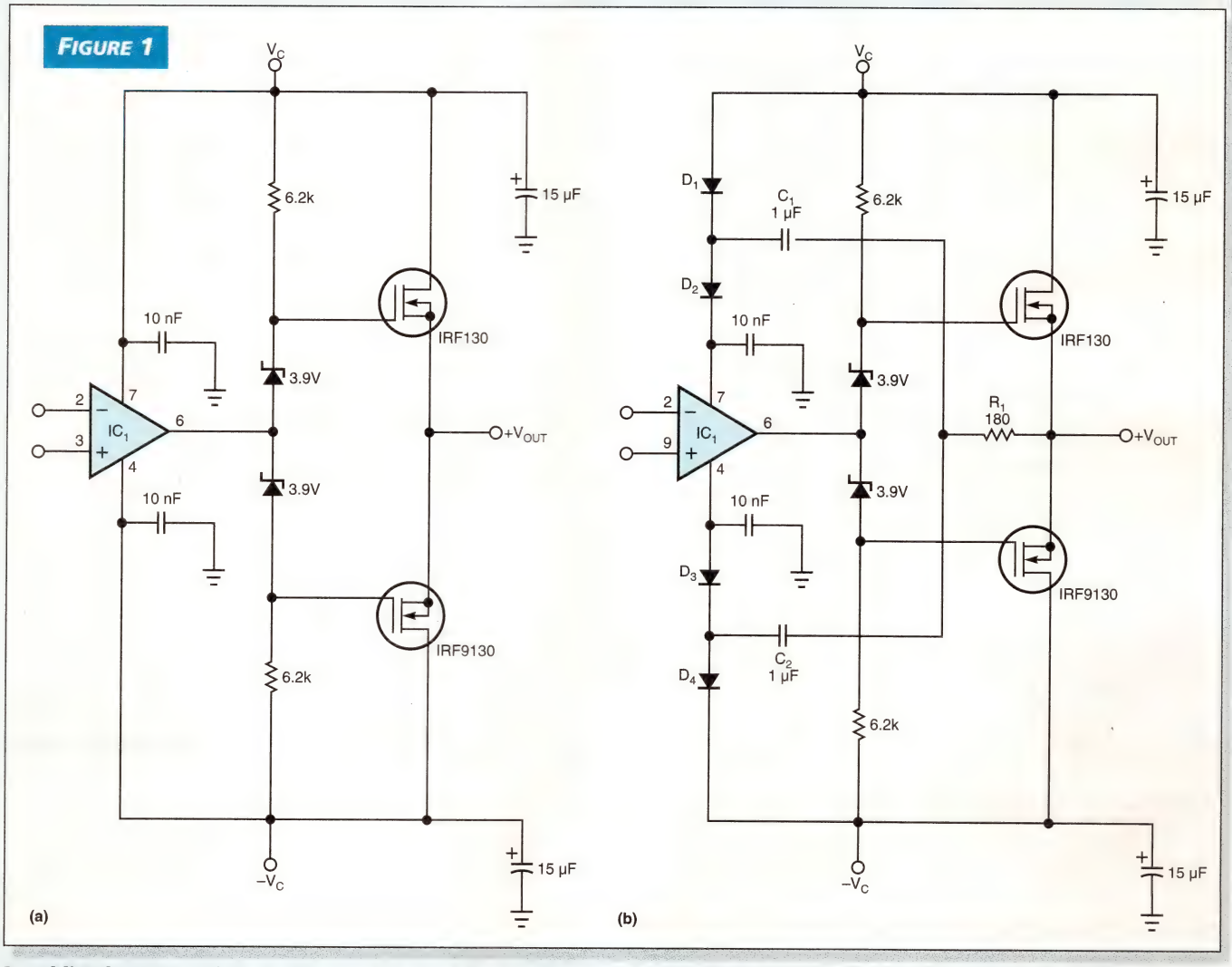
FIGURE 1



By adding bootstrapping components to the circuit in (a), which has a limited output swing, the circuit in (b) provides a transient rail-to-rail output swing.

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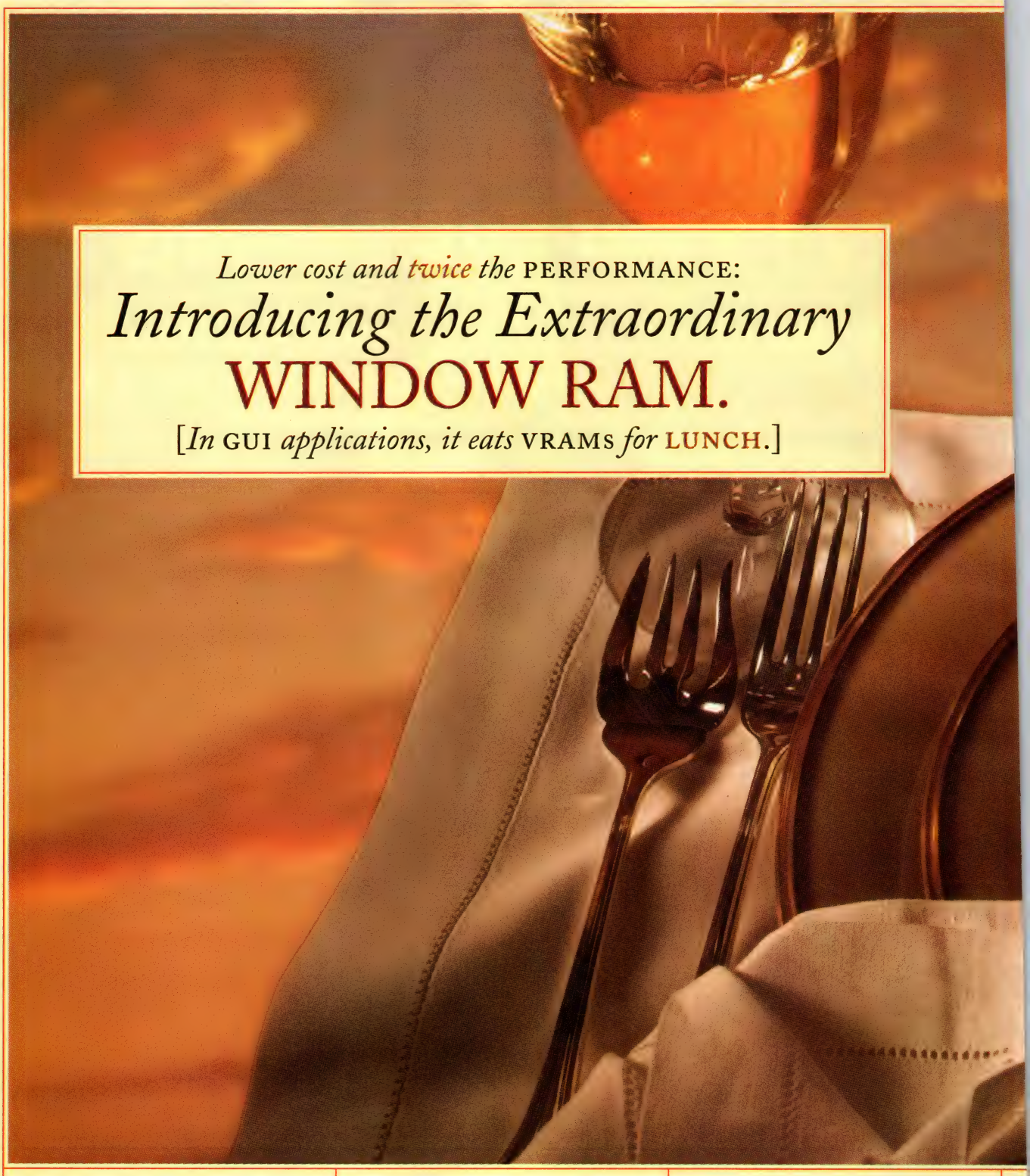

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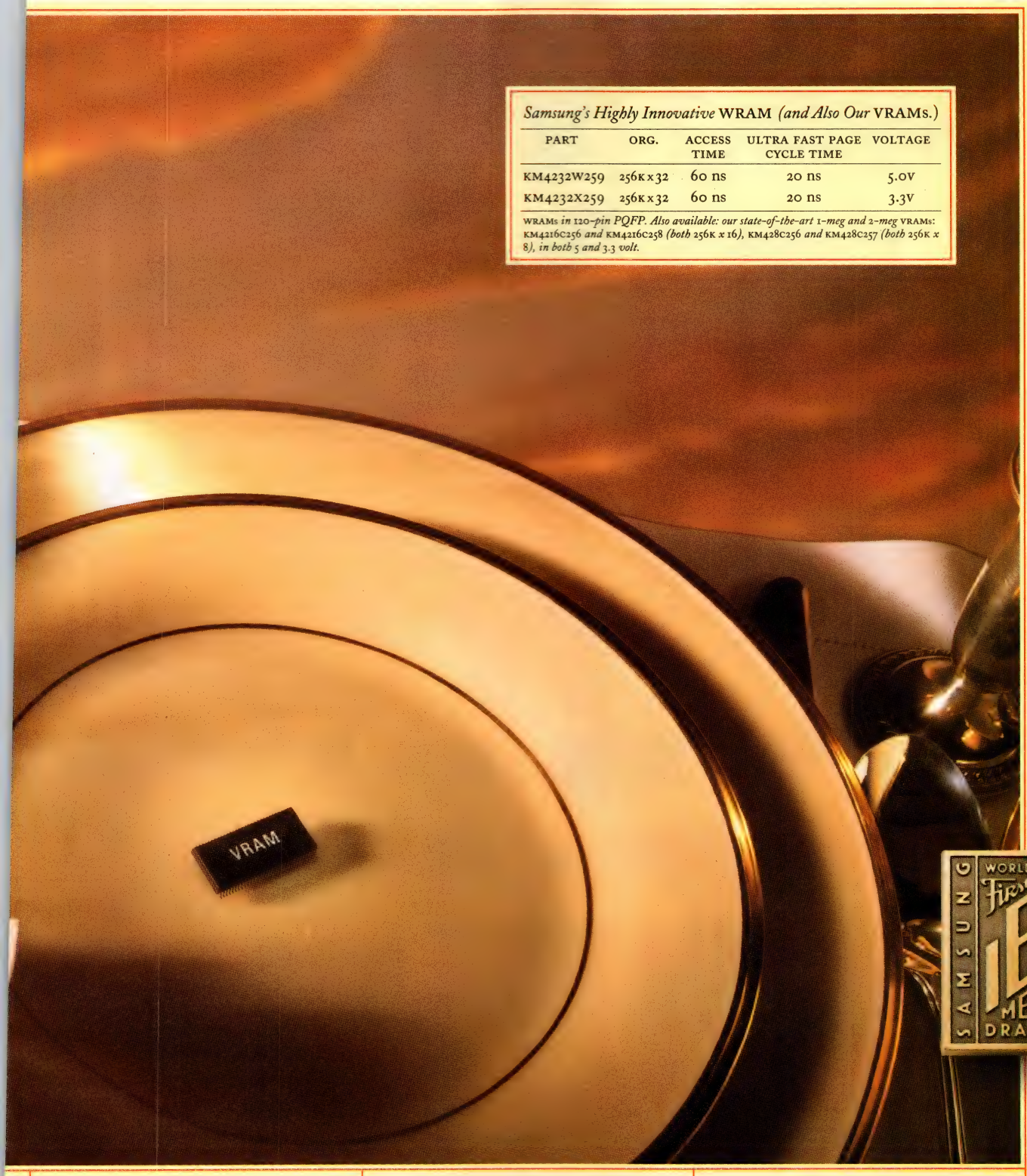

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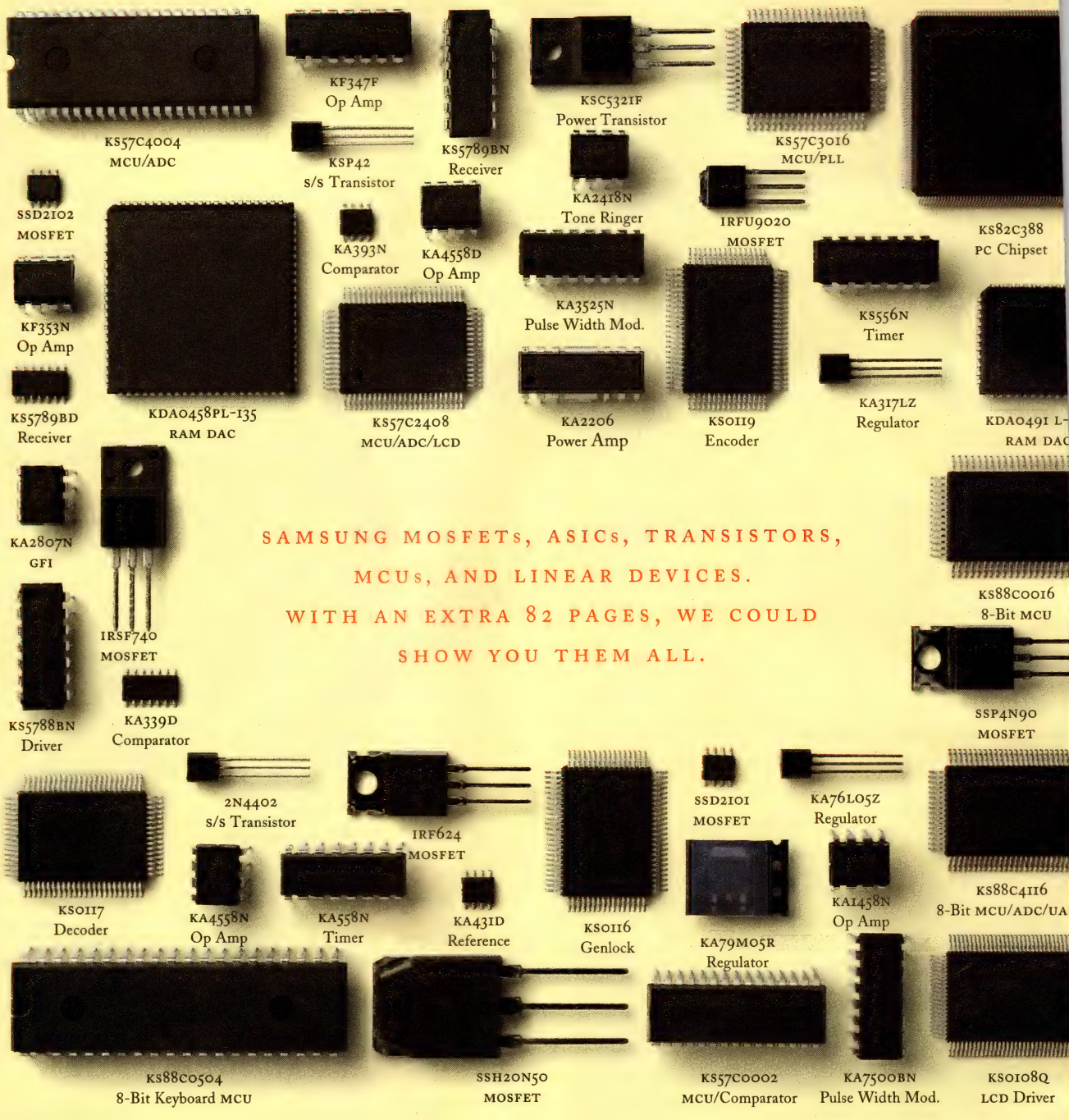

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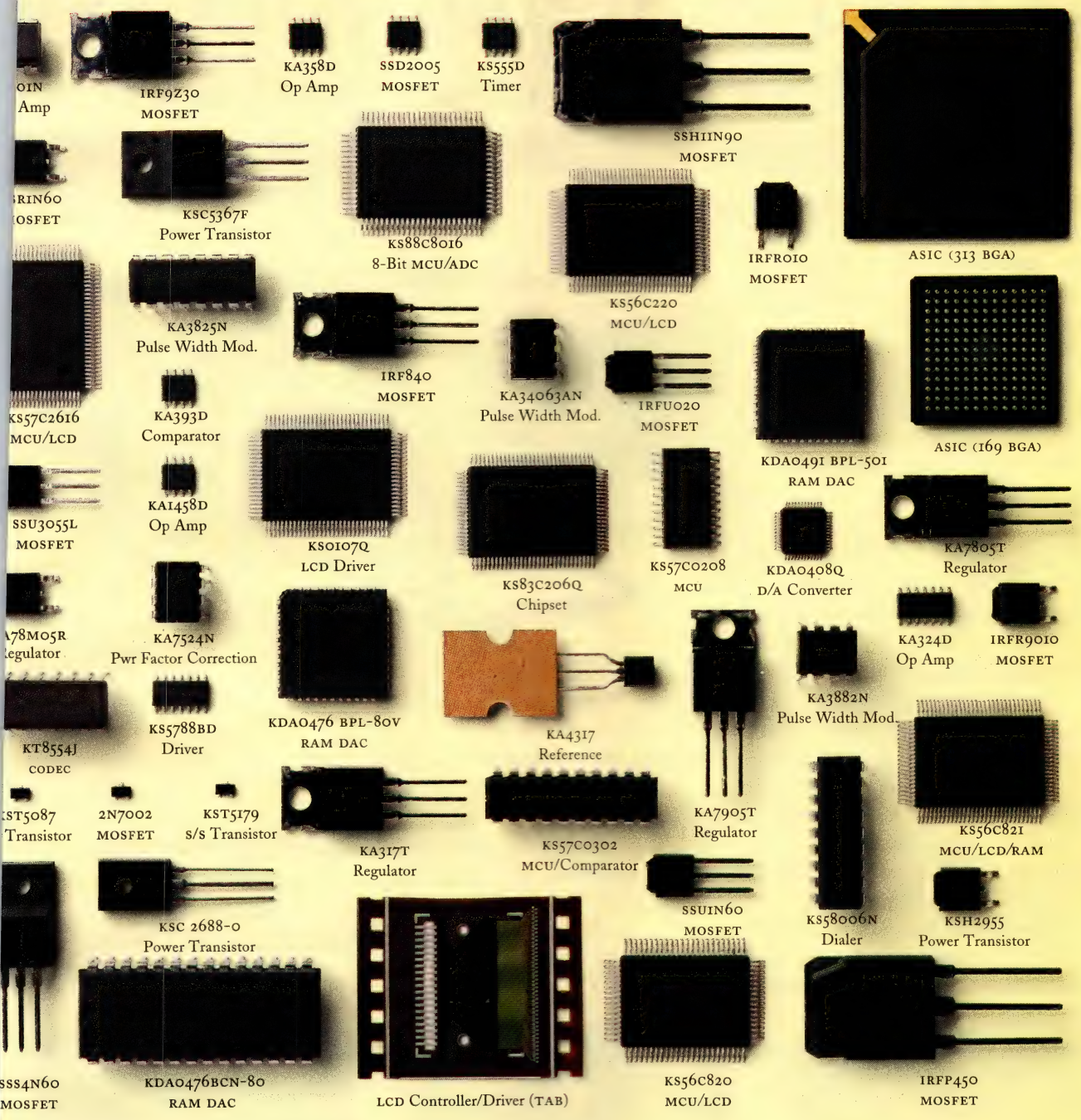

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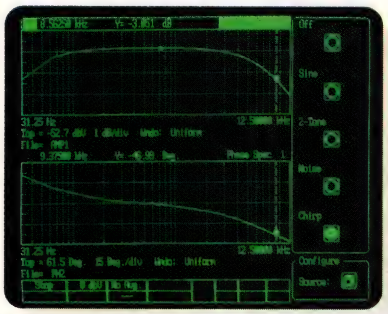

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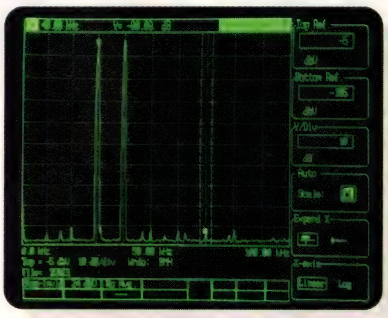

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CIRCLE NO. 103

To build data-acquisition systems that run from 5 or 3.3V, know your ICs

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Data-acquisition systems that take power from a single 3.3 or 5V supply share many design considerations with systems that run from ±15V. Some concerns are unique to low-voltage, single-supply operation, however. To avoid problems, you need a thorough understanding of the ICs you use.

Continued demands for lower power, lower cost systems increase the likelihood that your next mixed-signal design will operate from a single 3.3 or 5V power supply. Doing away with traditional ±15V analog power supplies can help you to meet your power and cost goals, but it also will eliminate some of your design options.

Fortunately, when you select a data-acquisition system's most critical component, the ADC, you have many low-voltage parts from which to choose. But after you pick an ADC, critical decisions still lie ahead. This article looks at how low-voltage ADCs, amplifiers, and other components work together in practical systems, and how you can avoid some of the most common problems that occur when you combine these functions in low-voltage equipment.

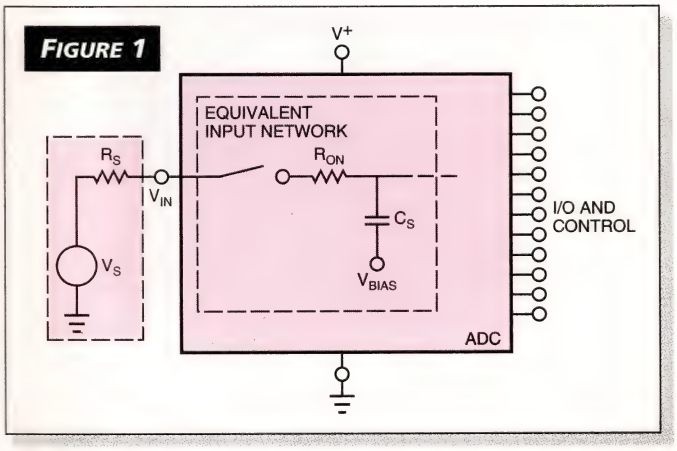
Most low-voltage ADC and DAS (data-acquisition system) chips are designed for easy analog and digital interfacing. The ICs' digital interfaces are generally compatible with popular microcontrollers, and the devices can almost always accept analog input signals that range from ground to the positive supply voltage; the span is set by an internal or external band-gap voltage reference. Virtually all ADCs that operate from 5V or less are CMOS devices that use arrays of switches and capacitors to perform their conversions. Although the architectural details vary from design to design, the input stage of this type of converter usually includes a switch and a capacitor that present a transient load to the input signal source. **Fig 1**'s simplified schematic shows how these input stages affect the circuits that drive them.

R_{ON} is not a separate component; it is the on-resistance of the internal analog switch. Sampling capacitor C_S connects to an internal bias voltage whose value depends on the ADC's architecture. In a sampling ADC, the switch closes once per conversion, during the acquisition (sampling) time.

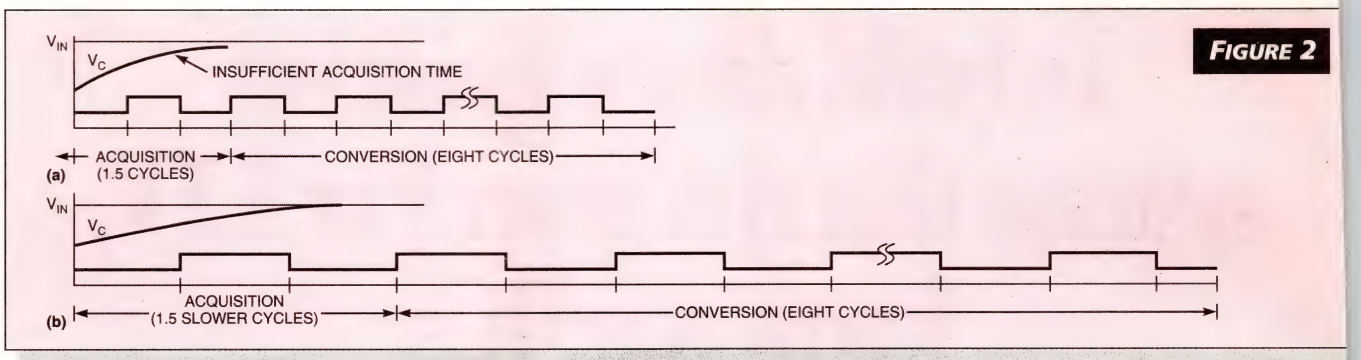
The on-resistances of the sampling switches range from about 5 to 10 kΩ in many low-resolution successive approximation ADCs to 70Ω in some multistep or half-flash converters. The capacitors can be as small as 10 pF in lower resolution successive-approximation converters and 100 pF or more in higher resolution devices.

When the sampling switch closes, the capacitor begins to charge through the switch and source resistances. After a time interval that is usually controlled by counters or timers within the ADC, the switch opens, and the capacitor stops charging. The time during which the switch is closed and the capacitor charges is called the "acquisition time." As long as the source impedance is low enough, the capacitor has time to charge fully during the sampling period, and no conversion errors occur. Most input stages are conservatively designed and can work properly at their rated speeds with a reasonable source resistance (1 kΩ is common). Larger source imped-

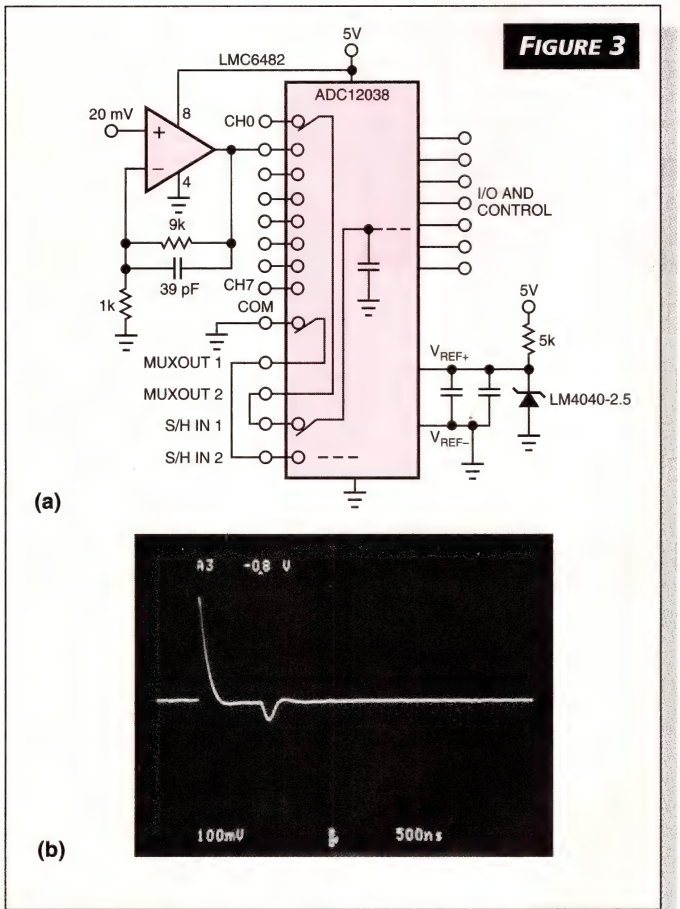
FIGURE 1



This circuit is a simplified version of the load that a low-voltage ADC presents to a signal source. The capacitor is normally referred to a bias voltage between ground and V+. When you connect a low-voltage ADC to a signal source, the source impedance, the on-resistance of the internal switch, and the sampling capacitor form a network whose time constant may be too long for accurate sampling of the input voltage.



A low-voltage ADC that is designed to operate properly with source resistances under 1 kΩ may encounter conversion errors if the source resistance increases to 2 kΩ (a). The larger source resistance prevents the voltage on the internal sampling capacitor from fully charging during the ADC's acquisition time (1.5 clock cycles in this case). When the source impedance is too high to allow accurate signal capture during the nominal acquisition time, you can often extend the duration of the acquisition window by slowing the converter clock (b). This approach slows conversion, however. A good alternative is to slow the clock only during acquisition and then return to the normal clock rate during the conversion itself.



Even a load that should be easy for an op amp to drive can disturb the amplifier if the load suddenly switches to the amplifier's output (a). This typical amplifier-ADC combination operates from a 5V supply. The scope photo (b), shows how the low-voltage CMOS op amp in (a) responds to the switching transients at the ADC input. The amplifier's output settles to within 1 LSB 1.5 μsec after the start of the ADC's acquisition period. Use the ADC's adjustable acquisition time to ensure that the acquisition window doesn't close until the amplifier settles.

ances slow the charging of the sampling capacitor and cause significant errors unless you take steps to avoid them.

Source resistance can be unsettling

When the source impedance is high enough to degrade the conversion accuracy, a simple remedy is to increase the acquisition time to allow the capacitor more time to charge. The acquisition time depends on the conversion technique and other ADC characteristics. Often, you can adjust the acquisition time externally. For example, many sampling successive-approximation converters are clocked devices that sample the input signal for a specific number of clock cycles. Although you can adjust these devices' acquisition time simply by altering the clock frequency, doing so is not always desirable, because slowing the ADC's clock also lowers the conversion speed. Assuming that the loss in conversion speed is acceptable, this technique can increase the acquisition time by as much as two or three orders of magnitude, depending on the ADC. Check the ADC data sheet to verify that the converter operates properly at a sufficiently slow clock frequency; leakage currents that discharge the internal capacitors and cause conversion errors if the clock is too slow dictate most clocked ADCs' minimum clock frequencies.

As an example, imagine that the ADC in **Fig 1** is designed to yield correct conversion results for source resistances less than 1 kΩ when using a 4-MHz clock. Signal acquisition takes 1.5 clock cycles, and conversion takes eight more, so the nominal acquisition-plus-conversion time is 375 nsec+2 μsec=2.375 μsec. If the source resistance increases to 2 kΩ, the nominal acquisition time is no longer sufficient. **Fig 2a** shows that at the nominal clock frequency, the sampling capacitor doesn't charge fast enough to ensure accurate conversions. If the system must operate properly with a 2-kΩ source, you must double the acquisition time to 750 nsec. An easy way to do this is simply to halve the clock frequency. This doubles the acquisition-plus-conversion time to 4.75 μsec and slows the throughput rate accordingly. In **Fig 2b**, the clock frequency is halved, and the capacitor can charge sufficiently during the acquisition time.

When conversion time is critical, you may not be able to cut the throughput rate in half to accommodate a high

source impedance. Instead, you can run the clock at full speed during conversions and slow it only during the acquisition period. In this case, the total acquisition-plus-conversion time becomes 750 nsec+2 μsec=2.75 μsec, a significant improvement compared with 4.75 μsec.

You can also eliminate the effects of high source resistance by using a buffer amplifier ahead of the ADC. This approach requires an additional component, but accommodates very high source impedances with little or no loss in sampling rate, especially if you use a CMOS amplifier. Low-voltage amplifiers have limitations of their own, but they are sometimes the only solution when signals originate in high-impedance sources.

The amplifier/ADC interface

A discussion of low-voltage data acquisition isn't complete unless it considers amplifiers. Operational amplifiers are nearly always present in data-acquisition systems, performing basic signal conditioning ahead of the ADC. Their interactions with ADCs affect system performance. Although many amplifiers are good at driving a variety of static loads, the switched nature of the ADC input stage can introduce problems with some amplifiers, especially the low-power, low-speed devices that are most likely to be used in 3 and 5V systems. Using the simple model of **Fig 1**, the load presented to the amplifier by the ADC input keeps switching abruptly between an open circuit and a series RC network connected to an internal voltage source. The op amp's response to the sudden load-current and impedance change depends upon several parameters. Among them are the device's gain-bandwidth product, slew rate, and output impedance.

Fig 3a shows a low-voltage CMOS operational amplifier wired for a closed-loop gain of +10 and operating from a 5V supply. It drives one of the inputs of an ADC12038, a 5V, 12-bit CMOS ADC with eight analog input channels. The ADC's input network comprises 1.6 kΩ of series resistance and 75 pF of capacitance.

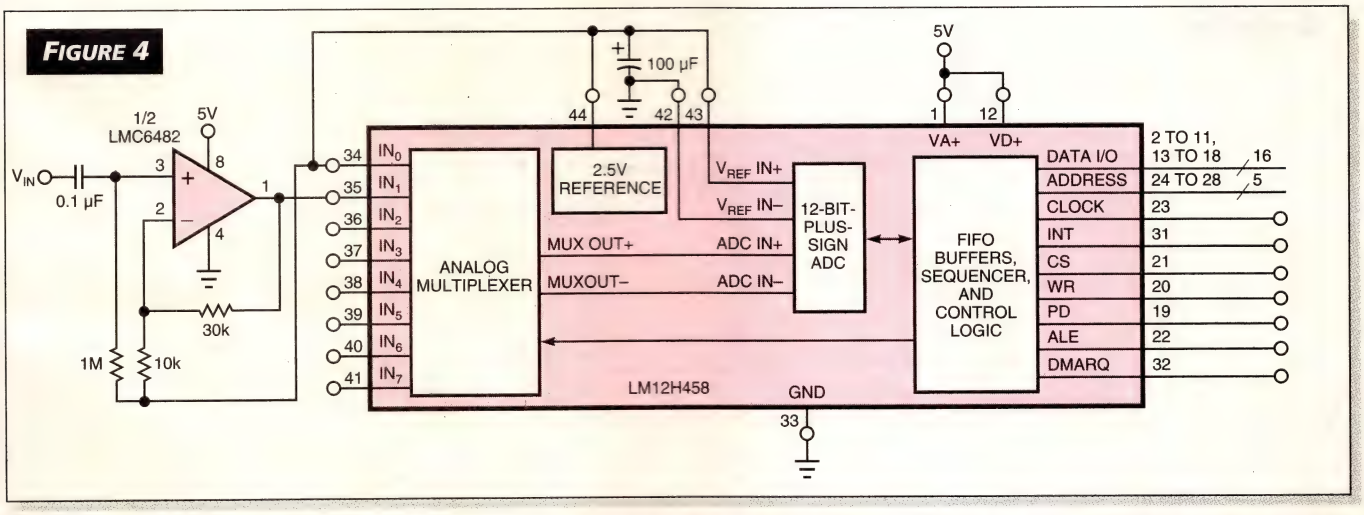
The oscilloscope photo in **Fig 3b** shows the output of the amplifier when it drives the ADC. In this case, the amplifier is an LMC6482 dual CMOS op amp with rail-to-rail input- and output-voltage swing. The first transient, which occurs when the input multiplexer switch closes, has a peak amplitude of 280 mV. The second, smaller transient, which occurs when the sampling switch closes, corresponds to the beginning of the ADC12038's acquisition period. The amplifier's output voltage settles to 1 LSB 1.5 μsec after this second transient. The worst-case settling for this amplifier-ADC combination for output voltages from 20 mV to 4.98V is 2 μsec. The settling waveform with a 3V supply looks similar, but the worst-case settling time increases by about 15%.

If an ADC samples an input signal for a period longer than the driving amplifier's worst-case settling time (roughly 2 μsec for the LMC6482/ADC12038 combination), the conversion results will be accurate. However, if the amplifier's output is still recovering from the load transient when the acquisition window closes, the voltage at the converter's input may differ significantly from the real input voltage, and the resulting conversion data will be wrong. Slow-settling amplifiers are unusable in many applications but can sometimes provide reasonable results with slow or low-resolution ADCs.

As in the case of high source resistances, you can improve system accuracy by increasing the ADC's acquisition time. You can do this by slowing the conversion clock. An alternative is to use an ADC or a DAS with adjustable acquisition time.

The ADC12038 (**Fig 3a**) has a signal-acquisition window that is adjustable from 1.2 μsec to 6.8 μsec (when using a 5-MHz clock), which allows for a wide range of amplifier settling times. For the LMC6482 operating at a gain of 10, setting the acquisition time to 2 μsec (10 clock cycles with a 5-MHz clock) provides adequate performance, and a new conversion can begin every 14.8 μsec, resulting in a 67.6-kHz sampling rate. If, instead, you use the ADC12H03, the high-

FIGURE 4



An operational amplifier with rail-to-rail output swing simplifies this amplifier-ADC circuit for digitizing ac signals with 13-bit resolution. Because the amplifier's output can swing to within a few millivolts of V+ and ground, you can use nearly all of the ADC's input dynamic range. If the amplifier's output swing limited, say, 500 mV from V+ and ground, you'd need a second reference to avoid losing 2 dB of dynamic range.

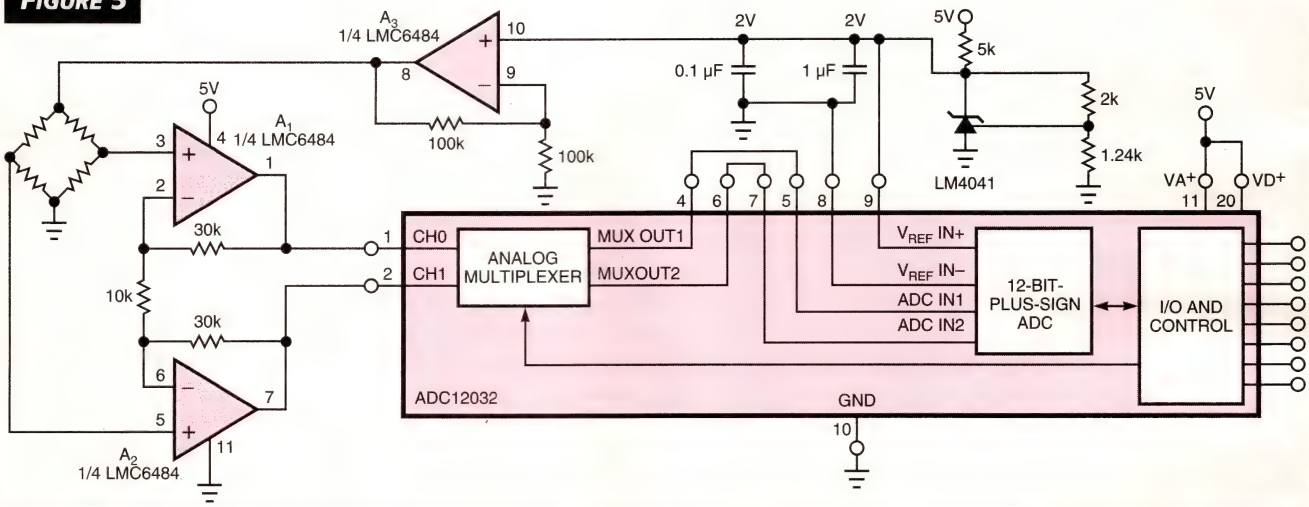
speed version of the ADC12038, the clock rate can increase to 8 MHz, which decreases the conversion time. If you select an 18-cycle acquisition window, the acquisition period will be 2.25 µsec, and the maximum sampling rate will be 99 kHz. Other ADCs and DAS chips with adjustable acquisition times (the LM12458 and LM12438 families, for example) can take advantage of this technique as well.

Which amplifier should you use? It depends on the speed, resolution, and accuracy you need. Look for amplifiers with gain-bandwidth products in the 1-MHz or greater range for 12-bit data acquisition at conversion rates between 50 and 100 kHz. Low-power, low-speed amplifiers are usually acceptable only if you're sampling slowly and can achieve a long enough acquisition time. The time required for the output to settle after a load transient is not something you find on most amplifier data sheets; you have to test the amplifier-ADC combination to verify that it works properly in your system.

Do you need rail-to-rail outputs?

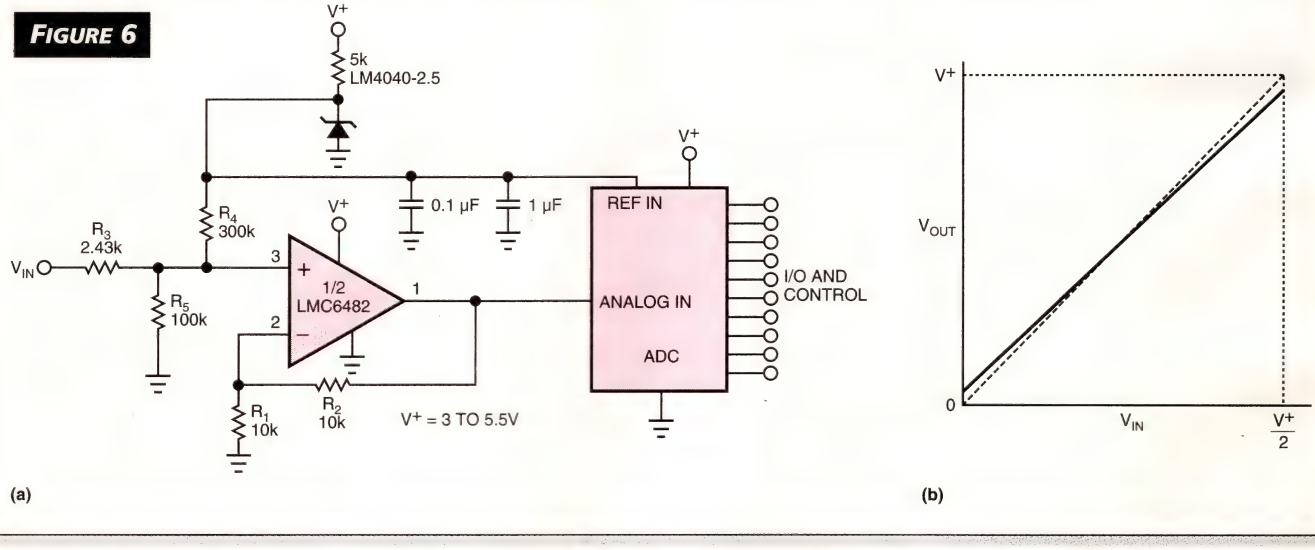
The amplifier that precedes the ADC conditions the input signal; it may buffer a high source impedance, provide gain or level shifting, or alter the transfer function in some nonlinear way to compensate for sensor characteristics. In a ±15V system, an amplifier whose output can swing to within a couple of volts of the supply rails may be perfectly adequate, but in a 3 or 5V system, the amplifier must swing much closer to the supplies. Do you need rail-to-rail output swing? Not always, but it's helpful in many applications.

FIGURE 5



In this circuit, low-voltage amplifiers A_1 and A_2 provide differential gain to the output of a load cell and differential drive to an ADC's differential inputs. A_3 doubles the 2V ADC reference to provide bias for the bridge.

FIGURE 6



When you can't afford to lose very-near-ground signals to offset and swing limitations, you can add some offset to the input signal (a). R_3, R_4, and R_5 reduce the ADC's nominal input range but increase the usable input range because they also reduce the range of signals applied to the amplifier input (b).

Fig 4 shows a simple amplifier circuit that provides gain to an ac signal at sampling rates up to 140 kHz. You can set the dc voltage at the amplifier's output to a convenient voltage near the half-supply point; in this 5V circuit, the output is biased at the 2.5V reference voltage. The circuit takes advantage of the DAS chip's differential inputs and sign bit to achieve 13-bit resolution. IN_0 and IN_1 are a differential input pair; IN_0 is connected to V_{REF}=2.5V. Input signals that swing above 2.5V have a positive sign bit; those below 2.5V have a negative sign bit. If the amplifier can swing to within 25 mV of ground and V+, you can use 99% of the ADC's full-scale input range. Using an amplifier whose output stage limits at, say, 500 mV, will lose 20% of the full-scale range and reduce the S/N ratio by about 2 dB unless you reduce the amplifier's gain and develop a second, lower reference voltage to drive the ADC's reference input pin.

In **Fig 5**, the output from a load cell drives a pair of amplifiers that differentially amplify the cell voltage. The differential output voltage from A_1 and A_2 drives the ADC's differential inputs. The reference voltage can match to the amplifiers' output swing. Because the LMC6484 amplifier can swing within a few millivolts of the supplies, a 2V reference works well. A_3 doubles the ADC's reference voltage to provide bridge bias. As in the ac-amplifier example, arriving at a practical design is easier if the amplifiers can swing very close to the supply rails, but it's not critical that they do so.

Living on the edge

Limited output swing causes more trouble when you need to work with input signals near ground. For example, a noninverting amplifier with a gain of 10 can take a 0- to 250-mV input signal up to 0 to 2.5V at the ADC's input. Virtually all low-voltage ADCs accept input voltages anywhere within the ADCs' supply rails, so a 3 or 5V ADC can easily handle a 0 to 2.5V input range.

Unfortunately, single-supply amplifiers can't produce usable signals closer to the supply rails than a few millivolts. If you need to digitize signals very near ground at 12 bits of resolution, your amplifier may not be up to the task. (The first code transition for a 12-bit ADC with a 0 to 4.096V range is at 0.5 mV.) In addition, if the amplifier's offset voltage is negative, you will be throwing away input signals that are too small to overcome the offset-voltage and output-swing limits.

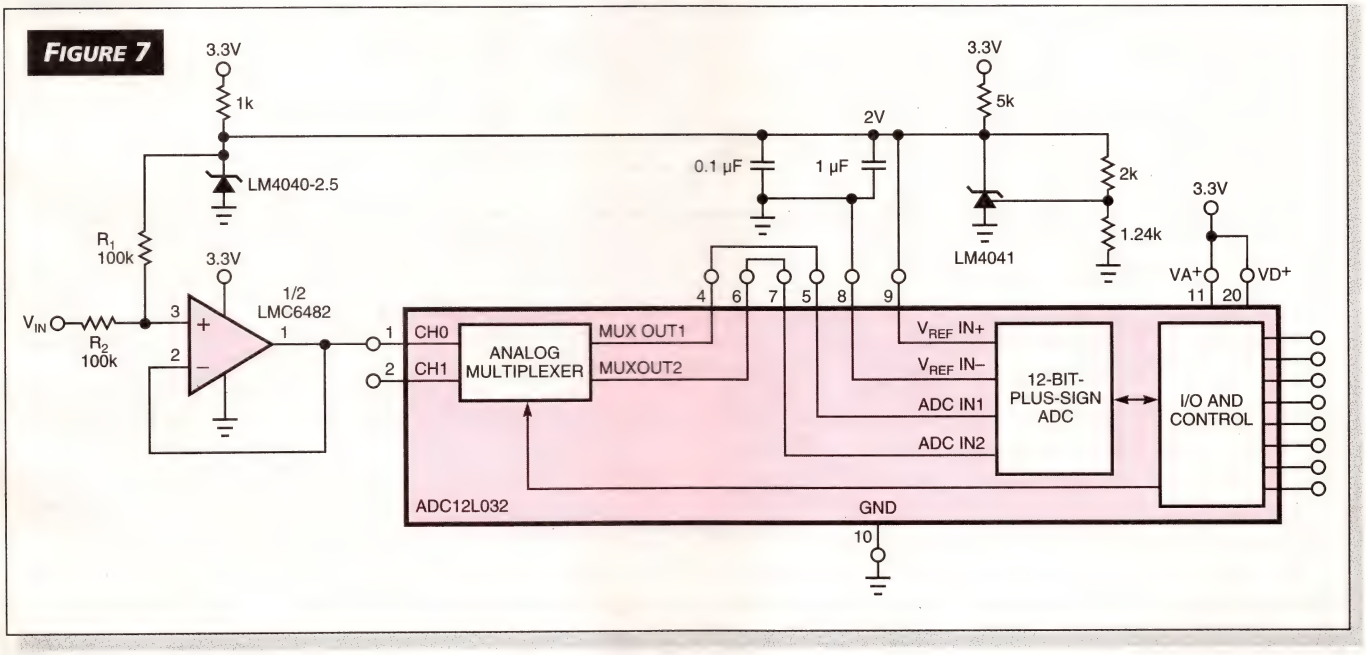
Fig 6 shows a simple way to recover input range lost to amplifier offset and output-swing limits. Resistors R_3, R_4, and R_5 shift the amplifier's output range up by 20 mV. Even when the input signal is at ground, the amplifier's output exceeds the output stage's limit voltage and is linearly related to the input.

Handling bipolar input signals

The ADCs discussed here have unipolar supplies and input ranges, but input voltages aren't always unipolar. Although it is uncommon to generate any negative or bipolar signals in a system that operates from a single positive supply, you may occasionally need to accept negative or bipolar signals generated outside of your system.

Fig 7 shows the simplest way to deal with these signals: A pair of equal-valued resistors is connected to V_{REF}, the amplifier's input, and the signal source. This circuit converts an input signal whose range is $\pm V_{REF}$ into an output with a range of ground to $+V_{REF}$; the network shifts the input voltage and divides the input signal by two. Input signals near ground shift up to $V_{REF}/2$, so they are always within the ADC's input voltage range. In this 3.3V system, the input voltage swing is ±2.5V. In a 5V system, the reference

FIGURE 7



A pair of resistors at the amplifier's input transforms a bipolar input signal into a unipolar one that can drive a single-supply ADC. The analog-input range is now $-V_{REF}$ to $+V_{REF}$. You can make this circuit work on a 5V supply if you substitute an ADC12032 for the ADC12L032. With a 5V supply, you can extend the input voltage swing to ±4.096V simply by using a 4.096V reference.

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voltage might be 4.096V, resulting in a ±4.096V input swing.

If you're interested in accurately converting input signals that reach all the way to $-V_{REF}$, you run into output-swing and input-offset-voltage-swing limitations. You can deal with these by slightly altering the resistor ratio or reference voltage to keep the minimum worst-case input voltage above the amplifier's limit voltage. Most of the time, an amplifier's input voltage should range from ground to $+V_{REF}$. But having an input common-mode range that extends to ground isn't necessary if you aren't interested in input signals that extend all the way to $-V_{REF}$.

In most applications, the resistors should be relatively large so that they won't attenuate your signal source; something in the 10- to 100-kΩ range is typical for R_1 and R_2. The op amp buffers the high source impedance to eliminate the effect of source impedance on acquisition time. An op amp with extremely low input bias current is best for this application. The LMC6482 is used here because of its extremely low input bias current and rail-to-rail input and output-voltage swings.

Remember that the matching of the resistors affects the accuracy of the overall circuit. When precision is critical, you'll need precision resistor arrays (available from Beckman, Caddock, and Allen Bradley), with two or more matched devices (0.01 to 0.05% matching and better than 15-ppm temperature tracking) in a single package.

System calibration

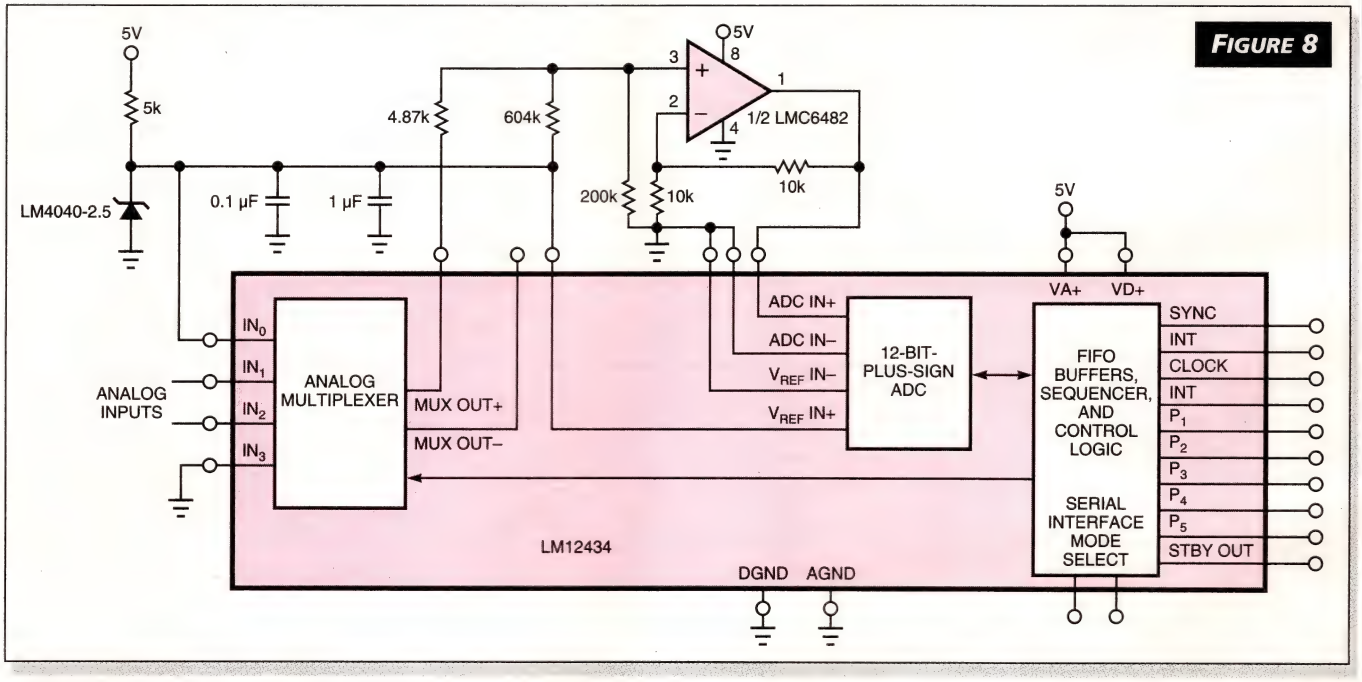
Whenever you perform analog signal processing ahead of your ADC, your signal-processing circuits can degrade the accuracy of your system. Amplifier offsets, reference errors and resistor tolerances can cause offset and gain errors in the output data. This is true in many systems but is especially true in low-voltage systems because amplifiers that work in those systems are rarely precision devices. In some systems a small amount of gain or offset error is inconsequential, but when the error budget is tight, you may need to perform some sort of calibration or error correction on the system.

Fig 8 provides an example of the concept of system-calibration. The circuit uses a simple but effective offset-calibration scheme. R_3, R_4, and R_5 provide offset shift. With typical op amps and resistors, several tens of millivolts of offset error can be present, and the precision with which R_3, R_4, and R_5 can be matched also affects the gain. The DAS chip's input multiplexer helps to perform calibration.

The calibration sequence begins by enabling the connection between IN_3 (ground) and MUXOUT+ and performing a conversion. This zero-scale calibration reading is called D_Z. Next, the connection between IN0, (V_{REF}), and MUXOUT+ is enabled to get full-scale reading, D_F D_F and D_Z can now be used to correct subsequent conversion results. Whenever a conversion is performed, the result, D_M (measured data), is adjusted to obtain the real input voltage within the resolution and accuracy limitations of the ADC:

$$V_{IN}=V_{REF}(D_M-D_Z)/(D_F-D_Z).$$

Switch on-resistance has a strong effect on the performance of this circuit. If the on-resistance mismatch is to affect the correction accuracy by less than 1 LSB, any mismatch between the analog switches' on-resistance should be less than $(R_4||R_5)/2^{n-1}$, where n is the converter's resolution in



Using an external multiplexer or the multiplexer switches in an ADC or DAS, you can measure the amplifier circuit's offset and full-scale errors and use them to correct subsequent readings. This circuit uses a 4-channel DAS chip. The circuit uses two of the input channels for calibration; the other two serve as the analog inputs. You can operate the circuit from a 3V supply by replacing the LM12434 with an LM12L434.

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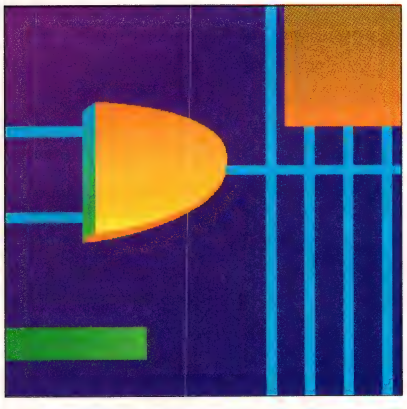

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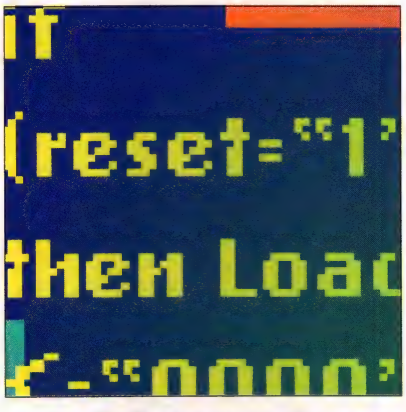

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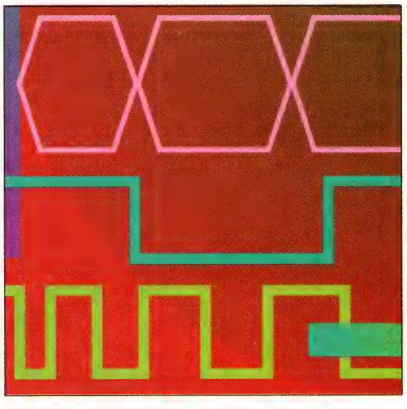

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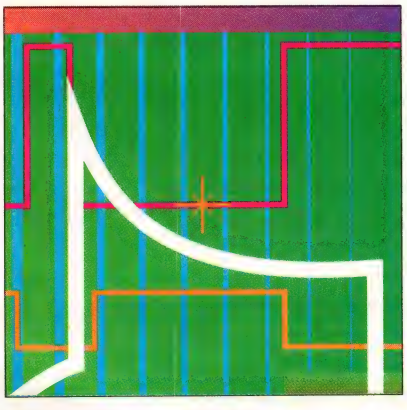

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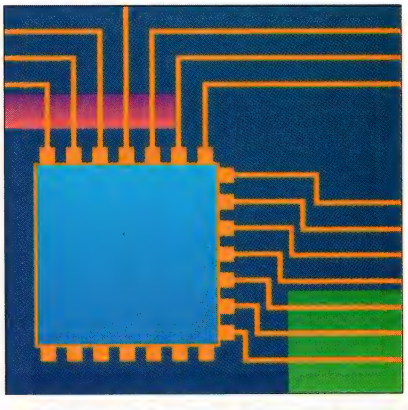

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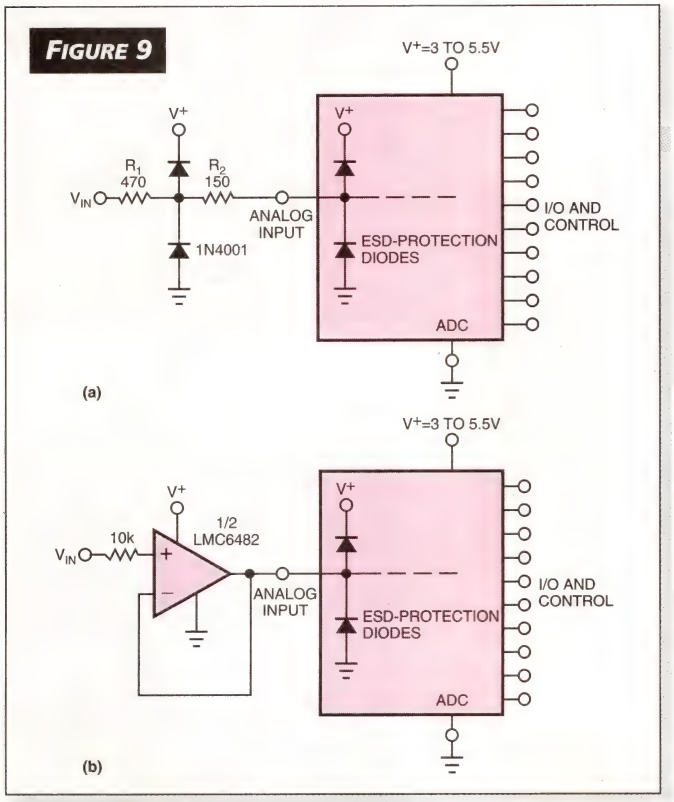
bits. For a typical 12-bit ADC, the on-resistance of the internal multiplexer switches might be on the order of 1.5 kΩ max. If the switches match to within 5% (75Ω), $R_4||R_5$ must be at least 150 kΩ, which might result in a value for R_3 on the order of 3 to 5 kΩ. When lower on-resistances are necessary, you can use an external multiplexer with lower R_{ON}.

You can modify the circuit of **Fig 8** for 3V operation simply by replacing the LM12434 serial DAS chip with its low-voltage version, the LM12L434. The technique is not restricted to DAS chips; it works with any multichannel ADC with MUXOUT and ADCIN pins.

When do you need input protection?

When a data-acquisition circuit's supply voltage is only 5 or 3V, you have abundant opportunities to overdrive the ADC's inputs. The lower the power-supply voltage, the more likely it is that a signal greater than the supply voltage will inadvertently drive the device.

When the analog input signal applied to a CMOS ADC exceeds the power-supply voltage, incorrect conversions, latch-up, or even permanent damage can result. Most ADCs



By using clamp diodes (a), relatively small resistors protect an ADC's input from large overdrives and avoid the long acquisition times often needed with high-value protection resistors. In (b), an amplifier makes an excellent protection device. Because it operates from the same 3V supply as the ADC, the amplifier can't overdrive the ADC's logic input. If its input bias current is low, the amplifier's input resistor doesn't add any dc errors. Watch out for noise, though; if the resistor is too large, its thermal noise will be significant at high gains.

begin to run into trouble with overdrive voltages of just a few hundred millivolts, while others can withstand several volts of overdrive.

When the ADC's analog inputs connect to the outside world, almost any input voltage can appear. One solution is to add clamp diodes to the circuit (**Fig 9a**). R_2, which limits the current into the IC, can be as small as 100 to 200Ω because the clamp diodes turn on at a voltage very close to the ESD-protection diodes' turn-on voltages (assuming the clamp diodes are silicon devices). R_1, which limits the clamp-diode current, depends on the maximum current rating of the clamp diode and the maximum expected overdrive voltage. For example, if the maximum possible input overdrive is 50V, a 500Ω R_1 limits the external clamp-diode current to less than 100 mA. This value is compatible with most CMOS ADC input stages and doesn't slow the charging of the sampling capacitor enough to affect conversion accuracy.

If your system includes amplifiers or other components to condition analog signals ahead of the ADC (and this is probably the case), you can often use these devices to protect the ADC's inputs. For example, a 5V CMOS operational amplifier can operate from the same 5V or supply as the ADC and, therefore, can't overdrive the ADC. The problem now becomes protecting the op amp from damage due to large input signals. Unlike a current-limit resistor at the input to the ADC, however, a resistor at the op amp's input pin doesn't affect conversion accuracy as long as the amplifier's input bias current is low. In fact, a CMOS op amp like the one in **Fig 9b** has virtually no input bias current (40 fA), so the primary error source is high-frequency roll-off due to the current-limit resistor and the input capacitance.

With a 10-kΩ input-protection resistor as in **Fig 9b**, the upper cutoff frequency is typically on the order of 8 MHz, which is much greater than the gain-bandwidth product of the amplifier. If you convert from bipolar to unipolar signals as in **Fig 7**, the level-shifting resistors protect the amplifier from overdrives, and additional resistors are unnecessary.

Some recent ADCs include built-in protection for overdrive voltages well in excess of the supply voltage. The ADC12038 in the circuit of **Fig 3** and the LM12434 in **Fig 8**, for example, can handle overdrives at least 5V beyond the supply voltage. Therefore, for limited overdrives, they need no protection at all.

When powering-down equals blowing up

If a system is designed for low power dissipation, chances are good that it operates from a 3 to 5V supply. It's also likely that the system uses some form of power management. A common approach to reducing power dissipation involves shutting down sections of the system that are not in use at a given time.

A simple technique is to shut off the power supply to the unneeded circuits. You can accomplish this conveniently using a voltage regulator with a shutdown logic input. When a system does not need the analog circuits, the microcontroller shuts them down via the voltage regula-

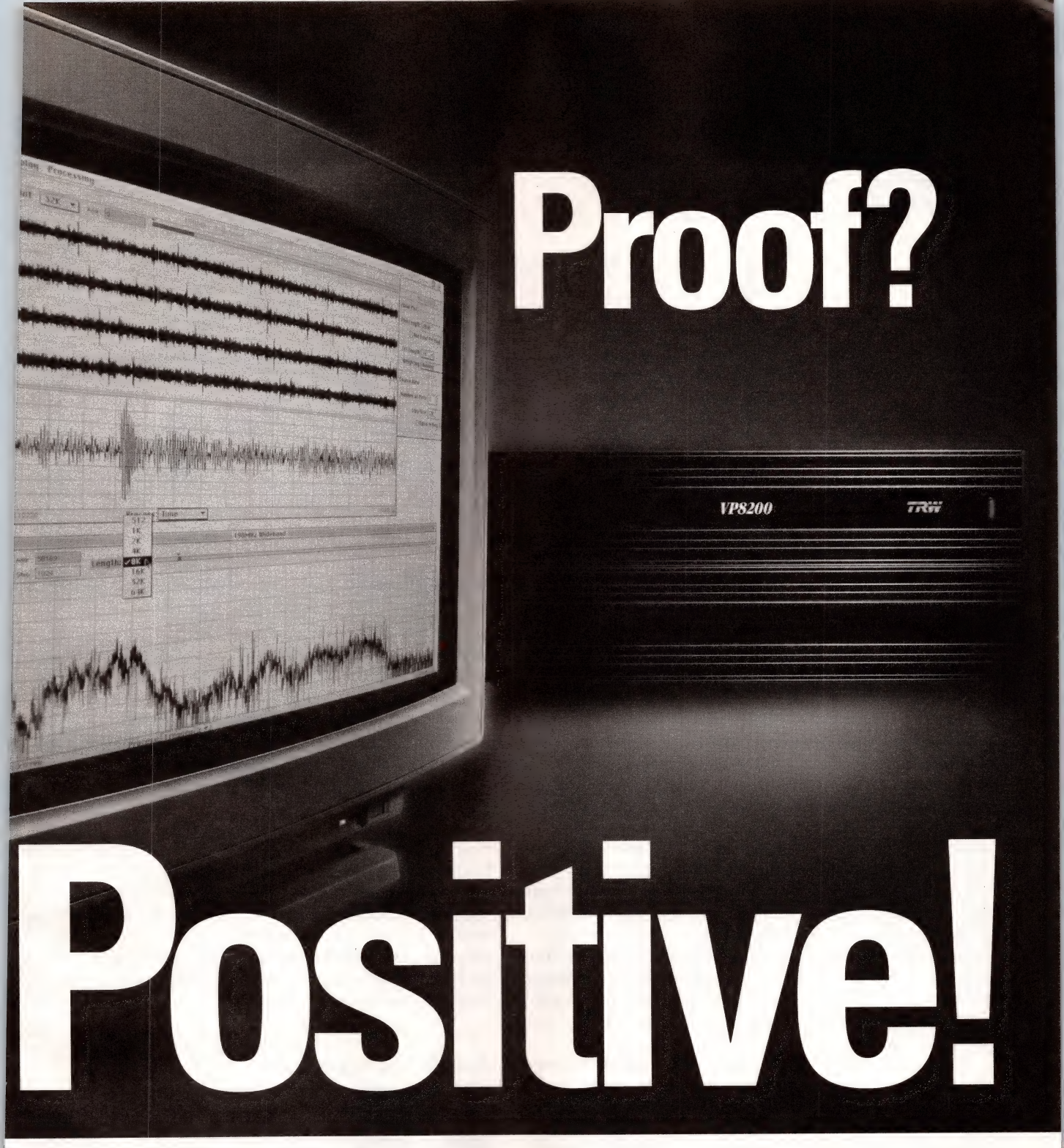


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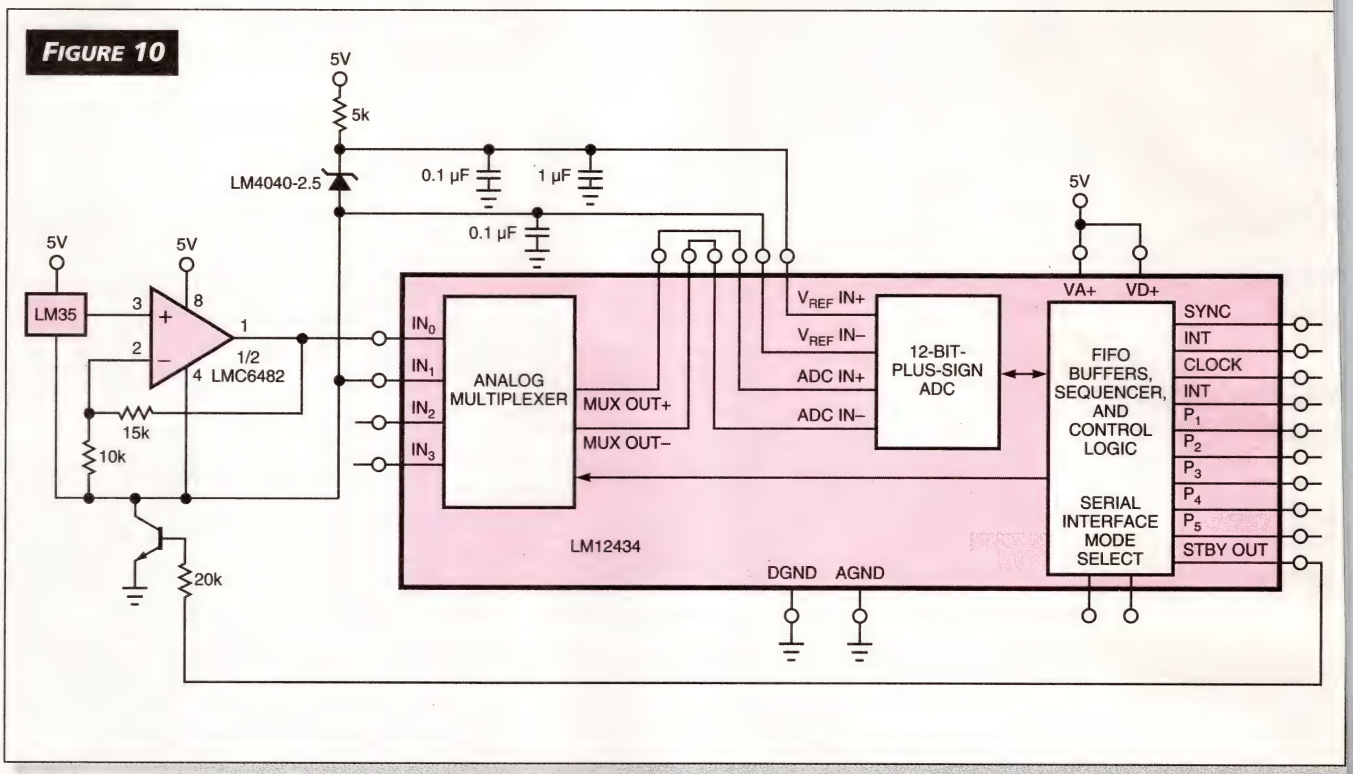
FIGURE 10



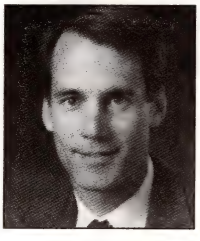
When you can shut down your ADC or DAS, you can reduce power drain between conversions without running the risk of overdrive by logic signals. In this temperature monitor, for example, when the DAS chip goes into shutdown mode, it also shuts down the temperature sensor, amplifier, and reference via its standby output pin and an external npn transistor. When you shut down the circuit, you reduce its power dissipation to only 50 mW.

tor's shutdown pin. The drawback to this approach is that the digital parts of the system are still active. If one of the ADC's digital input lines is pulled high by a digital circuit that remains powered up, that input can be damaged, or the IC may latch up because the logic signal exceeds V+, which is 0V when the power supply is shut down. In some systems, it is a simple matter to keep the digital circuitry from driving the ADC while its supply voltage is off, but this is not practical in every system, especially if the ADC connects to a bus.

Because of this problem and because shutting down a voltage regulator often requires additional components and circuit-board area, several recent ADCs include power-down functions on-chip. Either driving a shutdown pin to a specified logic level or issuing a software command through the ADC's I/O forces the ADC into a low-power state with its supply voltage still applied. Since the supply voltage is present, digital circuitry operating from the same supply can't overdrive the ADC during shutdown. An example appears in **Fig 10**. In this 0 to 100°C temperature monitor, the µP directly shuts down the LM12434 serial DAS chip. The npn transistor, which is driven by the DAS chip's standby output pin (STBY), shuts off the temperature sensor, amplifier, and 2.5V bandgap reference. The circuit, therefore, requires no additional lines from the microcontroller other than those that control the DAS.

When active, the DAS-amplifier-sensor-reference subsystem dissipates less than 43 mW. When shut down, the subsystem dissipates about 50 µW. When the circuit is active, the differential inputs on the DAS look at the amplifier output and reference with respect to the npn transistor's collector, thus eliminating any errors caused by the transistor's saturation voltage. By simply shutting off the converter and other analog components between conversions, you can achieve very low power dissipation, even with a relatively fast, high-performance converter. EDN

Author's biography



Kerry Lacanette is data-acquisition applications manager at National Semiconductor Corp in Santa Clara, CA, where he has worked for 16 years. Lacanette is responsible for defining data-acquisition products and designing circuits that use data-acquisition ICs. He holds BSEE and MSEE degrees from the University of California, Santa Barbara, and is a member of the Audio Engineering Society.

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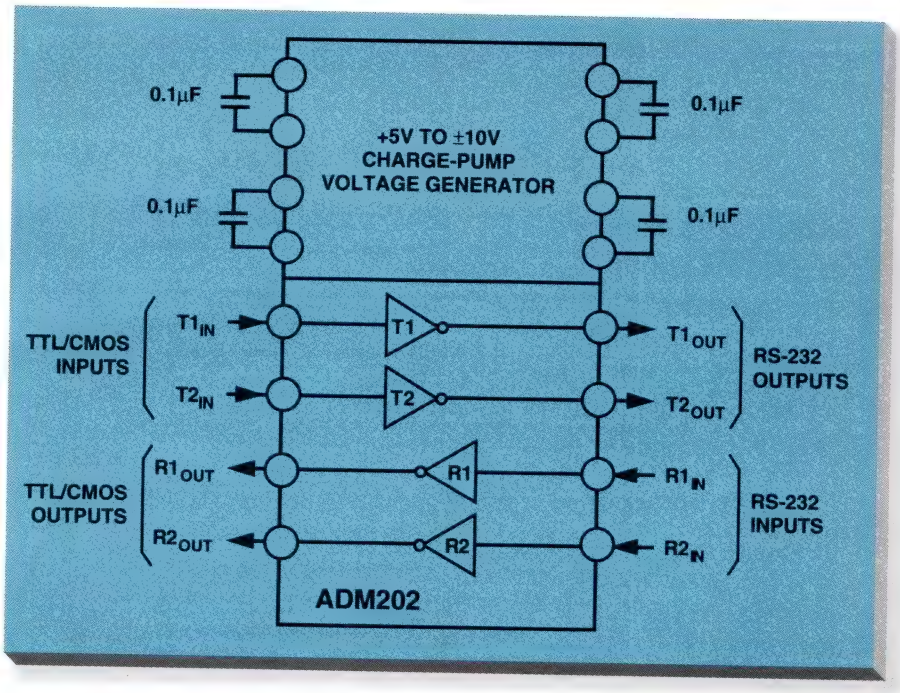
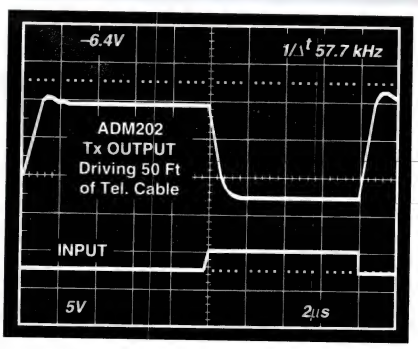


ADM202 KEY FEATURES

- 4 mA max I_{DD}
- Operates on single 5-V supply
- Industry standard pinout



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ADM5170/5180 KEY FEATURES

- Low power consumption
- Octal drivers/receivers
- 28-lead PLCC package

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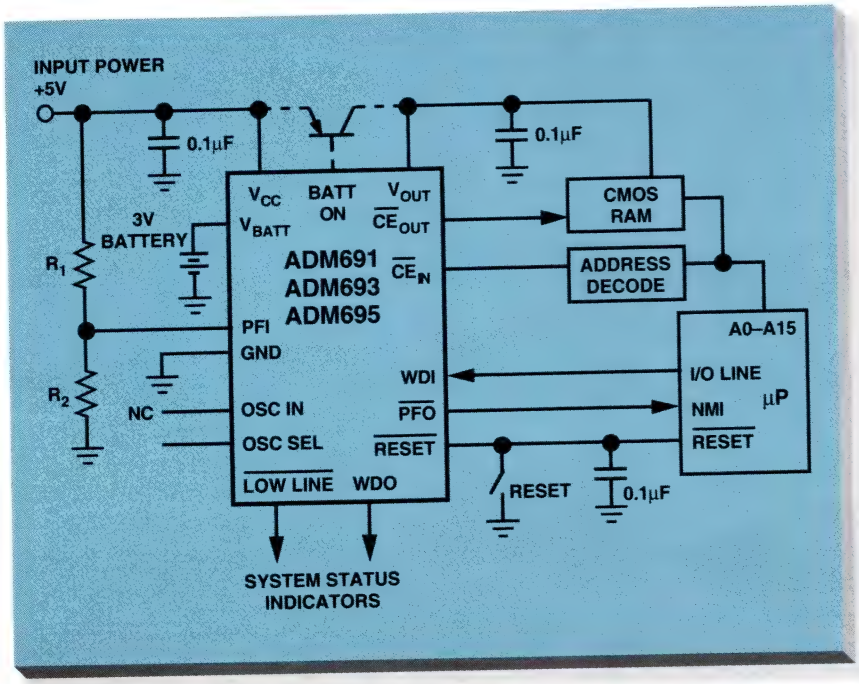

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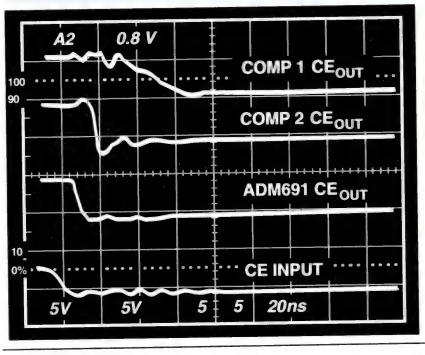

ADM691 KEY FEATURES

- 9 ns max prop delay
- Less than 2 mA max I_{DD}
- Switches battery currents up to 100 mA

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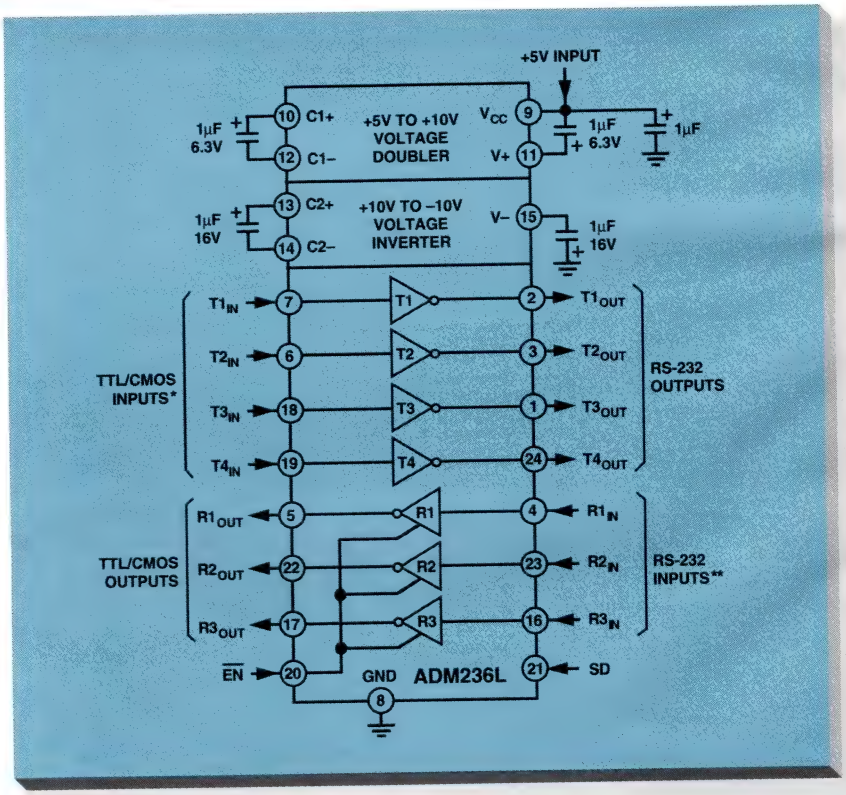


ADM232L KEY FEATURES

- 4 mA max I_{DD}
- Latch-up free
- Low cost

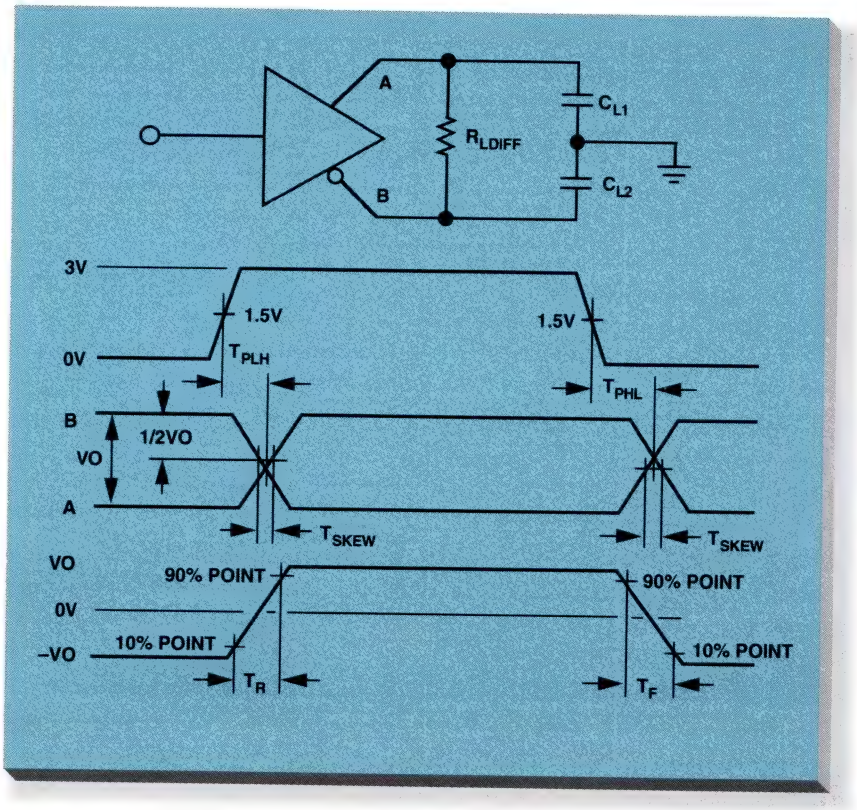
FOR DATA SHEETS OR SAMPLES

HIGH DATA RATE/LOW SKEW RS-485 CONSUMES ONLY 2.2 mA

For applications that require high speed and low skew, but with minimal supply current, investigate the ADM485 and ADM1485 from Analog Devices.

The ADM485 is a 5 Mbps, 2.2 mA single RS-485 transceiver in an 8-pin package. The ADM1485 blazes along at 30 Mbps, and still requires a miserly 2.2 mA. Both have typical 0 ns driver output-to-output bar skew, so you may relax your "skew budget" for cables and other devices.

Pricing begins at $1.24 for the ADM485, and $1.55 for the ADM1485.



ADM1485 KEY FEATURES

- 30 Mbps
- 2.2 mA max
- Zero output-to-output bar skew

3.3-V NOTEBOOK PC SERIAL PORT DRIVES 100 FEET CABLE WITH FULL RS-232 LEVELS AT 116 kBPS

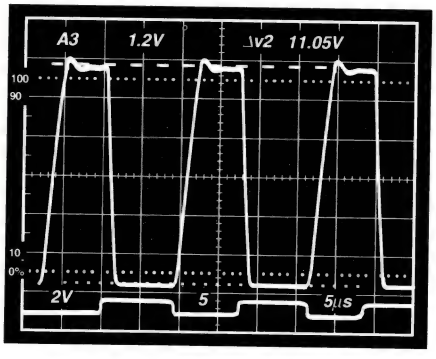
The new ADM560/1 complete serial port transceivers consume only 1.5 mA typical, but are capable of driving serial port mice and supporting 116 kbps data rates on 100 foot cables at 3.3 V.

The ADM560/1 feature maximum data rates of 230 kbps. Their digital inputs may be driven up to 5 V with a 3.3-V supply, allowing use in split-supply systems.

The ADM560/1 are pin compatible with xxx241, and are available in SSOP packages. Prices start at $2.10.

ADM560/1 KEY FEATURES

- 1.5 mA I_{CC} typical
- 230 kbps max data rate
- Drives serial port mice



Signal measured at receiver input when ADM560/1 used to drive 100 feet of RS-232 cabling at 116 kbps. Fully meets RS-232 levels while providing clean waveforms to ensure error-free communications.

LINEAR REGULATOR PROVIDES 3-V, 5-V AND VARIABLE VOLTAGE AT 100 mA

Analog Devices' new linear regulators, the ADM663A and ADM666A, feature the patented Tri-Mode system. This system allows you to select a pre-trimmed 3.3-V, 5-V or adjustable output voltage. Additionally, the regulators provide 100 mA current, thermal shutdown, ultralow power shutdown of 6 µA (typical) and many other industry-leading features.

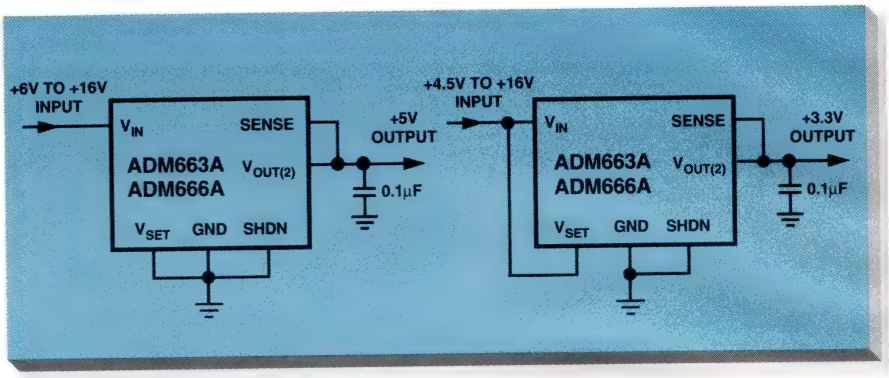
The ADM663A and ADM666A are ideally suited for applications requiring, for example, 9 V to 5 V or 5 V to 3.3 V at up to 100 mA with shutdown – using no external components and providing 5% accuracy.

Now you can achieve 3.3 V or 5 V with power fail warnings, shutdown, programmable current and other capabilities using only the tiny 8-pin SOIC package of the ADM663A/666A and a single 0805 body stability capacitor.

Pricing begins at $1.40 for the ADM663A, and $1.65 for the ADM666A.

ADM663/6A KEY FEATURES

- Pre-trimmed 3.3-V, 5-V or adjustable output voltage at 100 mA
- Low power shutdown of 6 µA (typical)
- 8-pin SOIC package



CHOOSE HIGHEST PRECISION/LOWEST NOISE OR LOWEST POWER WITH ANALOG DEVICES' REFERENCES

Whether you need the industry's highest precision/lowest noise 2.5-V voltage reference, or the lowest power 2.5-V or 5.0-V voltage references, Analog Devices can meet your requirements.

Analog Devices' AD780 is the highest precision 2.5-V voltage reference available, and can also provide 3.0-V output while maintaining industry standard pinout. It has a temperature coefficient of 3 ppm/°C, and initial accuracy of 1 mV over the entire industrial temperature range. The AD780 offers the lowest noise, 100 nV/$\sqrt{\text{Hz}}$, in its category. It also offers the lowest price, beginning at $3.30, of any high precision, low noise reference. The AD780 is available in various package options, including both surface mount and through-hole.

The REF192 and REF195 are the first two members of our new micropower precision voltage reference family. For portable or battery-powered applications, these references feature a low quiescent current of 45 µA (max), and 15 µA in sleep mode. The REF192 and REF195 provide 2.5-V and 5.0-V outputs, respectively, with initial accuracy of ±2 mV and temperature coefficient of ±5 ppm/°C.

The REF195 also features a low dropout voltage of 100 mV with a 1 mA load. Maximum load current is 30 mA for both references, allowing dual use as micropower regulators. Future micropower reference products will cover your complete reference needs for 3-V and 5-V systems. The REF19x reference pricing starts at a low $1.94.

AD780 KEY FEATURES

- Temperature coefficient of 3 ppm/°C
- Initial accuracy of 1 mV
- Noise 100 nV/$\sqrt{\text{Hz}}$

REF192/195 KEY FEATURES

- Low quiescent current of 45 µA max, 15 µA in sleep mode.
- Low dropout voltage of 100 mV with a 1 mA load
- Pricing starts at a low $1.94.

ANALOG DEVICES

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Fax: (617) 326-8703

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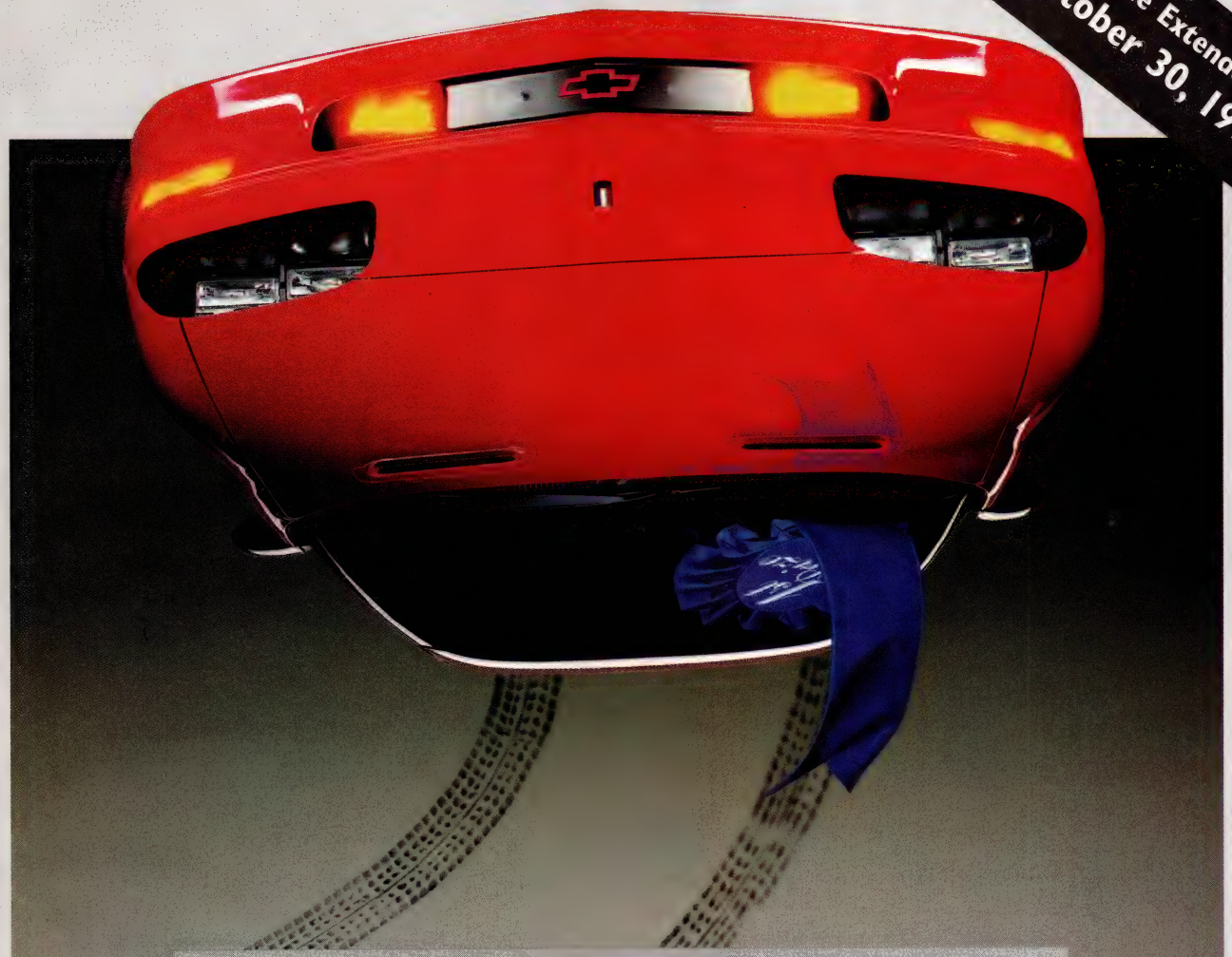

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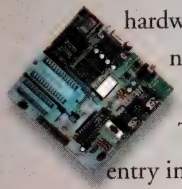

Together, they give you winning designs. Which is why you should be sure to enter the exciting Philips Dream Machine Design Contest. Just submit a design to us using the 8XC750 or any Philips 80C51 microcontroller derivatives by September 30, 1994. If it turns our judges on their heads, you could win the Camaro or a color or monochrome laptop computer.

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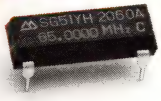

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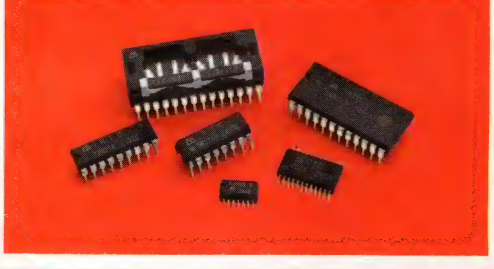
RTC-658X 8 bit parallel bus, 114 bytes SRAM, battery holder.
RTC-659X 8 bit parallel bus, 114 bytes SRAM, alarm, battery holder.



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CIRCLE NO. 75

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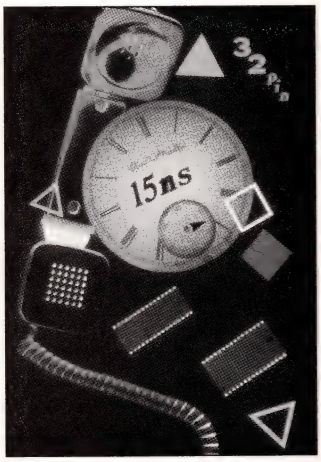
Three-phase brushless motor controller in surface-mount package. The Si9979CS controller integrates a high-side drive and low-voltage regulator functions. The controller provides commutation from Hall-effect sensors, letting you use 60 or 120° spacing. Other features include inputs for direction, quadrature selection, PWM and braking control with cross-conduction protection, current limiting, and undervoltage lockout. The device handles motor currents from 1 to 5A. When combined with the company's Little Foot power MOSFETs, the total board space is less than 3.5 in.^{2} for controlling 20 to 40V motors. The Si9979CS costs $7.09 (1000). **Siliconix**, Santa Clara, CA. (408) 988-8000.
Circle No. 414

Video op amp features a 3-dB bandwidth of 110 MHz at a gain of 2. The op amp drives double-terminated 75Ω coaxial cable to video levels and has a TTL-compatible disable function. Enable and disable times are 75 nsec. The device operates on any supply voltage from ±5 to ±16V and consumes 7.5 mA, regardless of supply-voltage level. You can connect outputs of multiple devices for multiplexer applications. Differential gain and phase are <0.01% and 0.01°, respectively, at 500Ω. The EL2166 comes in eight-pin plastic DIP and SOIC packages and costs $2.90 (1000). **Elantec Inc**, Milpitas, CA. (408) 945-1323.
Circle No. 415

Digitally controlled potentiometer has audio log taper. The X9314 audio log taper E^{2}POT provides 32 steps arranged in an audio log taper. Chip-select, direction, and increment signals select the output level, and the setting is stored in EEPROM. End-to-end resistance is 10 kΩ. $0.86 (10,000). **Xicor Inc**, Milpitas, CA. (408) 432-8888.
Circle No. 416

DSP offers on-chip flash memory. The FlashDSP 1616 executes 50 MIPS at 5V and 30 MIPS at 3V. The on-chip 12k-word flash memory lets you quickly load, test, and reload development software. Because the FlashDSP behaves the same as the ROM-coded version, system performance does not change when you use the flash-based DSP for development and then change to a ROM-based version for production. The FlashDSP 1616 costs $1000 (10) and is available now. Development kits with three engineering samples, software, and hardware-development tools will be available by year-end for $20,000. **AT&T Microelectronics**, Allentown, PA. (800) 372-2447.
Circle No. 417

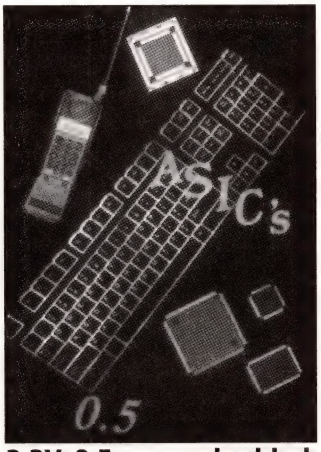


3.3V SRAM available in TSOP. The 15-nsec, 256-kbit M5MV278DVP-15 is configured as a 32k×8-bit device. The standby current is 100 µA max (10 µA typ) in power-down mode. Active current is 90 mA max (80 mA typ). The high speed, low power, and small package suit the device to cache-memory systems in portable computers. In addition to the 28-pin TSOP, the device comes in DIP, SOJ, and SOP packages. $6. (1000). **Mitsubishi Electronics America Inc**, Sunnyvale, CA. (408) 730- 5900.
Circle No. 418

64-bit RISC processor offers 150-MHz operation, family price reduction. The Orion R4600 Mips RISC µP family offers lower prices than previous versions and a 150-MHz version. The device suits Unix and Windows NT applications. Prices are $175 for the 100-MHz version, $250 for the 133-MHz version, and $325 for the new 150-MHz version. All versions are available. **Integrated Device Technology Inc**, Santa Clara, CA. (800) 345-7015.
Circle No. 419

DSP-based codec handles four speech channels. For use in private-branch-exchange and central-office switches, the SICOFI-4 PEB 2465H handles as many as four analog subscriber channels. The chip interfaces four analog telephones to the digital-switch environment, including encoding, decoding, and pulse-code-modulation circuitry. Programmable DSP functions include impedance matching to eliminate telephone-line echo, transhybrid balancing to eliminate echoes and signal losses in the subscriber-line interface circuit, and two programmable filters. Production quantities will be available in the third quarter and cost $12.70 (10,000). **Siemens Components Inc**, Cupertino, CA. (800) 777-4363, ext 274.
Circle No. 420

High-power semiconductor family uses ISOTOP package. The ISOTOP (SOT-227) package offers a 2500V isolation rating, a parasitic inductance of <5 nH, and a thermal resistance of 0.27°C/W in a 5-cm^3 volume. The package suits 500W to 3-kW industrial applications and works with the company's new TMOS family of MOSFETs, ultrafast rectifiers, and Schottky rectifiers. The TMOS devices have $R_{DS(on)}$ values from 5.5 to 80 mΩ and voltage ratings from 100 to 500V. The MTE-215N10E costs $20 in production quantities. **Motorola Semiconductor Products Sector**, Phoenix, AZ. (602) 244-3071.
Circle No. 421

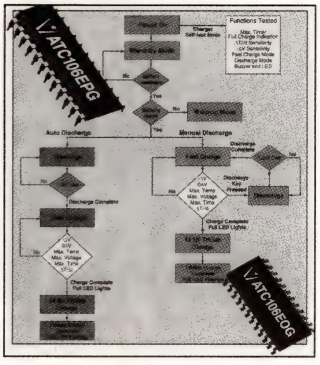


3.3V 0.5-µm embedded-cell ASICs have 170-psec gate-access time. The M6010X devices have a gate-usage rate of approximately 70% and a maximum of 1 million available raw gates. The company offers embedded high-speed synchronous or asynchronous, single-port RAM with up to 256 kbits per block. A 512-word×32-bit synchronous RAM has a 3.7-nsec worst-case access time. Multiport RAM is also available. The clock-distribution system can drive 5000 flip-flops with worst-case skew of <300 psec. The ASICs have a PLL with lock ranges selectable to 40 to 120 or 120 to 180 MHz. **Mitsubishi Electronics America Inc**, Sunnyvale, CA. (408) 730-5900.
Circle No. 422

Two-chip set handles 486 system logic and X-bus peripheral control. The VT82C496 system-controller chip includes a CPU and a local-bus interface, a cache controller with write-back and write-through for caches

from 32 kbytes to 1 Mbyte, a page-mode DRAM controller, a synchronous ISA bus controller, an integrated power-management unit, and an embedded VL bus IDE controller. The other chip in the set, the VT82C406MV IXP X-bus peripheral controller, includes a multiclock generator, a keyboard controller, a real-time clock, and miscellaneous functions. The Pluto chip set is available now and costs $18 in volume. **Via Technologies Inc**, Fremont, CA. (510) 683-3300.

Circle No. 423



µP-based fast battery charger uses special features for NiCd and NiMH batteries. The ATC106 battery-charging IC uses industry-standard techniques, $-\Delta V$ and $\Delta T/\Delta t$, for NiCd batteries. Automatic or manual discharging is also available. For safety, the IC measures maximum temper- ature and maximum voltage during the charge cycle. The IC does not limit the number of batteries being charged, and it accommodates either PWM or linear-power supplies. Because NiMH batteries do not always show a peak voltage when being fast-charged, the charger IC stops charging if the voltage remains unchanged or exhibits a zero ΔV after a period of fast charging. The charger also stops trickle charging NiMH batteries after 15 hours to avoid damage. The ATC106 includes self-test and costs $3.50 (1000). **Shoreline Electronics Inc**, Santa Clara, CA. (408) 987-7733.

Circle No. 424

2-to-1 video multiplexer has 210-MHz bandwidth at 1.4V p-p signal level. The MPC104 multiplexer has two identical open-loop buffer amplifiers offering 79-dB channel crosstalk and 86-dB off-channel isolation at 30 MHz. Differential gain-and-phase errors are 0.03% and 0.01°, respectively. Switching transients are +13 and −4 mV. The 1-pF typ output capacitance lets you assemble multiple multiplexers into large crosspoint fields. Performance is specified for ±5V supplies. $4.94 (100). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111.

Circle No. 425

Low-cost 5V, 16-bit ADC combines on-chip modulator, decimator, reference, and clock. The two-channel AD1877 features a fourth-order modulator, a three-stage decimator, a voltage reference, and a clock divider. Minimum dynamic range within the 20-Hz to 20-kHz bandwidth is 92 dB, and minimum signal-to-noise is 88 dB. The converter interfaces directly to standard µPs and DSPs. Available in a 28-pin SOIC, the AD1877 starts at $10 (1000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1428.

Circle No. 426

Op amps offer high speed and low noise. The CLC426 uses a voltage feedback architecture to provide a 230-MHz gain-bandwidth product with noise specifications of 1.6 nV/√Hz and 2 pA/√Hz. The op amp has a 400-V/µsec slew rate and settles to 0.05% in 16 nsec. The CLC426 is internally compensated for gains of two or more. The CLC428, a unity gain-stable-dual op amp, is also available. Prices start at $3.95 (1000). **Comlinear Corp**, Fort Collins, CO. (303) 226-0500. **Circle No. 427**

Three-chip set for notebook computers includes PCMCIA and X-bus controllers. The three-chip set includes the VT82C425 system controller for CPU and local-bus interface, DRAM control, ISA bus control, power management, and local bus IDE control; the VT83C465 PCMCIA socket controller for full implementation of two PCMCIA 2.0 sockets; and the VT82-C406MV X-bus peripheral controller, including multiclock generator, keyboard controller, and real-time clock. The Diana chip set costs $20 in volume. **Via Technologies Inc**, Fremont, CA. (510) 683-3300.

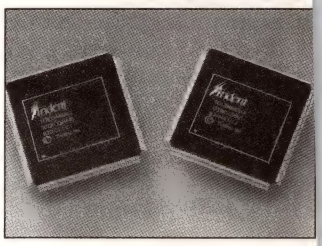
Circle No. 428

256kx16-bit DRAM features 100-Mbyte/sec page-mode data-transfer rates. The µPD424210A 4-Mbit DRAM supports clock speeds as high as 50 MHz with zero wait states. Samples are available now for $22, and mass production is expected in the fourth quarter. **NEC Electronics Inc**, Mountain View, CA. (800) 366-9782. **Circle No. 429**

3.3V SRAM family features access times down to 8 nsec. The µPD43xx32 family of 32kx32-bit CMOS SRAM is suited for use as secondary cache with high-speed µPs such as Intel's Pentium and Motorola's PowerPC. The memory family provides burst read and write in either Pentium- or linear-burst sequences. Pipelined and nonpipelined flow-through versions will be available. Expect samples in the fourth quarter of 1994 and full production in the first quarter of 1995. $50 (100). **NEC Electronics Inc**, Mountain View, CA. (800) 366-9782.

Circle No. 430

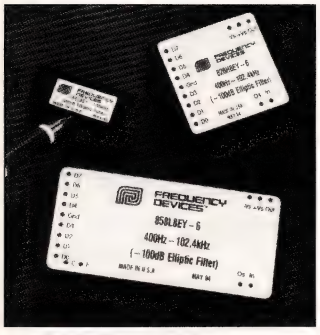
6-bit quadrature digitizer combines quadrature demodulation with A/D conversion. The MAX2101 accepts input signals from 400 to 700 MHz and pr vides adjustable gain for u to 40 dB of dynamic rang Each baseband may be fi tered using the include fifth-order Butterworth lo pass filter, variable from 1 to 30 MHz. The device als includes a programmabl counter for variable sampl rates and a signal-detectio function. The baseban sample rate is 60M sam ples/sec. Available in a 100 pin MQFP, the MAX210 costs $17.95 (1000). **Maxim Integrated Products**, Sun nyvale, CA. (408) 737-7600 ext 6087. **Circle No. 431**



32- and 64-bit GUI accelerators have live-video capability. The DRAM-based graphical user interface (GUI) accelerators include on-chip, 16-bit VESA advanced-feature connector DACs to provide live video. The chips allow the display of both full-screen and windowed full-motion video in noninterlaced 1024x768-pixel resolution using ½ Mbyte of DRAM. The 32-bit TGUI9440AGi includes an on-chip 108-MHz pixel clock and RAMDAC to display a 1280x1024-pixel image at 60 Hz noninterlaced. The 64-bit TGUI9660XGi uses an on-chip 135-MHz pixel clock to display a 1280x1024-pixel image at 75 Hz noninterlaced. The 32-bit chip costs $17 (OEM), and the 64-bit chip costs $27. **Trident Microsystems Inc**, Mountain View, CA. (415) 691-9211. **Circle No. 432**

12-bit ADC with sample-and-hold in 8-lead SOIC package. The converter uses three-wire serial I/O and consumes 20 µA at a 1k-sam-

ple/sec conversion rate. The converter operates from 3V supplies and is suitable for battery-power applications. When not converting, power consumption drops to 1 nA. The LTC1285 uses differential inputs, and the LTC1288 has a two-channel multiplexed input. $6.22 (1000) in plastic DIP and $6.63 (1000) in SOIC. **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 433**



Active filters provide –100-dB attenuation with low noise. A line of fixed and programmable linear-active filters provides high attenuation, and noise and distortion are low enough for use with 16-bit ADCs. The filters are factory-tuned to a user-specified corner frequency or an 8-bit tuning range from 1 Hz to 102.4 kHz. Lowpass filter types include Butterworth, Bessel, elliptic, and constant delay. Butterworth and elliptic filters are also available for highpass filtering. The D68 fixed-frequency filters start at $120 (1000), and the programmable-frequency 828 and 858 filters start at $275 (100). **Frequency Devices Inc**, Haverhill, MA. (508) 374-0761. **Circle No. 434**

Source-routing transparent interface for token-ring chip sets. The MU9C8148 SRT interface works with token-ring chip sets and the company's LAN content-addressable memory, providing a 128-entry instruction buffer that holds as many as seven downloadable filtering and purging routines. The interface meets IEEE standards and provides address-filter rates of 150,000 frames/sec for minimum-length frames. $30 (1000). **Music Semiconductor**, Colorado Springs, CO. (719) 570-1550. **Circle No. 435**

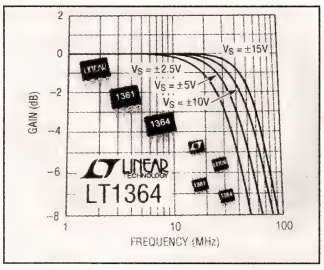
ICs provide building blocks for digital-communication networks. The STC104 uses the DS-link serial protocol developed by the vendor and now being adopted as an IEEE standard. Each chip has 32 DS-link inputs and outputs connected through a 32x32 crossbar switch that lets you route data streams from all inputs to all outputs simultaneously. Each input link has its own programmable routing engine that lets the chip handle 200 million packets/sec. The STC101 Parallel DS-link adapter provides an interface between the serial DS-links and external systems, such as buses, peripherals, and µPs. The STC104 costs $200, and the STC101 costs $20 in OEM volumes. **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300. **Circle No. 436**

Digital CMOS clock chip has 300-psec delay. The Equality 6600 clock-chip family have 10 adjustable outputs from 30 to 170 MHz. The chip uses digital techniques instead of voltage-controlled oscillators and PLLs to generate the clock signals. Pin-to-pin skew is 250 psec. $18 (500). **PLX Technology Inc**, Mountain View, CA. (415) 960-0448. **Circle No. 437**

RGB-to-NTSC/PAL analog encoder drives RGB monitors directly. The AD721 includes a pin-selectable encode or bypass mode. 100-MHz triple-video amplifiers with a gain of 2 can drive 75Ω reverse-terminated loads. The monolithic encoder provides the necessary lowpass filters and delay lines and operates from ±5V supplies. Suitable for applications such as PC-video plug-in cards and multimedia systems, the device provides composite video output with 0.1% differential gain and 0.1° differential phase errors. The 29-pin PLCC costs $6.25 (10,000). **Analog Devices Inc**, Wilmington, MA. (617) 937-1248. **Circle No. 438**

Transceiver chip set aims at 2.4-GHz wireless applications. The TQ9205 amplifier/switch front end provides transmit and receive switching configured for half-duplex operation at both the antenna and filter ports. The receive path contains a low-noise amplifier, and the transmit path contains a 100-mW power amplifier. The TQ9206 RF up/down-converter contains mixers, buffers, and an on-chip VCO for tuning over the 2.400- to 2.483-GHz band. The buffered output may be connected directly to the divider input of a PLL synthesizer. $9.77 (10,000). **Triquint Semiconductor Inc**, Beaverton, OR. (503) 644-3535. **Circle No. 439**

Monolithic 900-MHz GaAs down-converter operates off single 5V supply. The AWR0900 down-converter includes an oscillator and image filter and has a 3-dB noise figure and a 15-dB conversion gain. Low-power consumption makes the device suitable for battery-powered systems. $5 (1000). **Anadigics**, Warren, NJ. (908) 668-5000. **Circle No. 440**



High-speed op amps offer dc accuracy and low power consumption. The LT1361/62 voltage-feedback dual/quad op amps have a 50-MHz gain-bandwidth product and slew at 800 V/µsec, yet consume only 4 mA per amplifier. Maximum input-offset voltage is 1 mV. The LT1364/65 have a 70-MHz gain-bandwidth product, 1000-V/µsec slew rate, and 1.5-mV maximum input-offset voltage and consume 6 mA per amplifier. Differential gain is 0.06%, and differential phase is 0.04° when driving a 150Ω load. The LT1361 and LT1364 dual op amps start at $3.37 (1000), and the quad op amps start at $5.88 (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 441**

Nine-line active SCSI terminator works with 3V systems. The UCC5614 active SCSI terminator works with 3 to 5V systems and features a selectable 110Ω and 2.5-kΩ termination mode. Channel capacitance is 2pF. $2.90 (1000). **Unitrode Integrated Circuits Corp**, Merrimack, NH. (603) 424-2410. **Circle No. 442**

SRAM modules offer 2x512kx8-bit capacity. The EDI9F81025C-BPC CMOS SRAM module is a 36-pin SOIC package available with 70-, 85-, and 100-nsec access times. The memories are available in standard or low-power versions with data retention at 2 or 3V. Prices start at $346 (100) for the 100-nsec version. **Electronic Designs Inc**, Westborough, MA. (508) 366-5151. **Circle No. 443**

Wide and deep FIFO buffer provides color pixel formatting. The GT-24001 color pixel formatter comprises three 32-bit-wide by 1104-location-deep synchronous FIFOs. Although usable as a 33-MHz dual-port SRAM-based FIFO, the device includes features such as data packing and the use of a planar mode to reduce frame buffer memory by 25% in color printers, scanners, and copiers. The planar mode stores each color in a separate address space. $89.75 (5000). **Galileo Technology Inc**, San Jose, CA. (408) 451-1400. **Circle No. 444**

Hard-disk-drive read channel features low-power operation. The CXA1771R hard-disk-drive read channel requires 80 mA when fully powered in the read mode, 50 mA in the write mode, and 10 mA during standby. The read channel is capable of 32-Mbit/sec data transfers and operates from 3.3 to 5.5 V. Packaged in a 64-pin VQFP, the IC costs $15 (1000). **Sony Electronics Inc**, San Jose, CA. (408) 432-0190 **Circle No. 445**

SHORTS

The MAX662A improved 12V supply for flash memories has a 185-µA quiescent current, a 1-µA shutdown current and delivers 30 mA from a 4.75V input without inductors. From $1.81 (10,000). **Maxim Integrated Products**, (408) 737-7600, ext 6087. **Circle No. 446**

The AD600 and AD602 dual-channel variable-gain amplifiers and the single-channel AD603 are now military-qualified. Duals start at $52.50 (100), and the AD603 starts at $35 (100). **Analog Devices Inc**, (617) 937-1428. **Circle No. 447**

The following ADCs and voltage references have received standard military drawing numbers: AD87-1SD/883B, AD871SE/883B, AD87-2SD/883B, AD872SE/883B, AD67-4BTE/883B, AD757SE05/883B, and AD780- SQ/883B. **Analog Devices Inc**, (617) 937-1428. **Circle No. 448**

The ADC4322B 16-bit sampling ADC digitizes at 2M samples/sec, has no missing codes, and operates from –25 to +85°C. The hybrid costs $1194 (100). **Analogic Corp**, (508) 977-3000. **Circle No. 449**

Weitek Corp is lowering the price of its SPARC Power µP. The device, a CPU upgrade for SPARCstation 2 and IPX workstations, now costs $1200 with an installation kit and $995 for additional devices, with discounts for 100-piece orders. **Weitek Corp**, (408) 738-8400. **Circle No. 450**

Analog Devices has introduced a number of improved second sources with competitive prices: the ADM202, 222, 232A, and 242 dual RS-232C transceivers; the ADG441, 442, and 444 quad SPST switches; the ADG406, 407, and 426 16-channel multiplexers; and the ADM663 and 666 linear regulators. **Analog Devices**, (617) 937-1428. **Circle No. 451**

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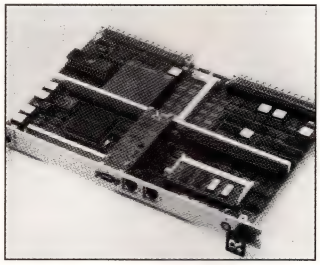
Multibus II CPU and I/O-controller board operates at up to 100 MHz. The CP 486/CBx offers a choice of processors ranging from the 33-MHz 486DX to the 100-MHz 486DX4. Memory modules let you populate the board with up to 32 Mbytes of DRAM. A CBX 16-bit memory-expansion interface lets you create I/O subsystems within a Multibus II system, using the company's digital- and analog-I/O cards. The board also accepts iSBX modules. Prices start at $3552 for a 33-MHz 486 with 8 Mbytes of DRAM. **Concurrent Technologies Inc**, Champaign, IL. (217) 356-7004.
Circle No. 467

VME-based FDDI adapters have OS-9 and Internet support package. The PT-VME600 adapter works with multimode optical fiber and provides reliable and secure data transmission between nodes. The PT-VME602 node adapter for unshielded twisted-pair category 5 cable takes advantage of existing wiring and helps reduce the cost per node. The PT-VME600 starts at $4195, and the PT-VME602 starts at $3095. The OS-9 Internet support package is available on all of the company's FDDI node adapters. **Performance Computer**, Rochester, NY. (716) 256-0200.
Circle No. 468

Emulator board converts the Motorola 68HC0-5P8EVS system for real-time in-circuit emulation. The EVSK1-ICE recreates the 68HC705K1 interrupt function and 64-bit personality EPROM subsystem in hardware for real-time emulation in target systems. The interrupt function provides external-level triggering or edge-triggering interrupt capability on the IRQ and PA0-PA3 pins. $295. **Wytec Co Inc**, Bloomingdale, IL. (708) 894-1440. **Circle No. 469**

VMEbus board is compatible with the Sun SPARCstation 5. The CPU-5CE uses a microSPARC II processor and delivers performance comparable to that of the SPARCstation 10 Model 40, according to the manufacturer. Onboard memory can range from 8 to 64 Mbytes of DRAM. The board includes a full range of I/Os, including fast SCSI, Ethernet, floppy disk, parallel port, serial and keyboard/mouse port. Software for the processor includes Solaris 1.1 and 2.3. Wind River Systems' VxWorks is available for users requiring a real-time operating system. Including 16 Mbytes of memory, the 6U VME board costs $4995. **Force Computers Inc**, San Jose, CA. (408) 369-6000.
Circle No. 470



VMEbus communications controller provides high-bandwidth serial communication channels. The SBCC-1 communications-controller board provides four high-bandwidth and three low-bandwidth-serial-communication channels. The board includes support for eight communication protocols, including HDLC, LAPB, X.25, Ethernet, ISDN T1/E1, and X.21. The four serial communication channels operate autonomously, allowing simultaneous operation of different protocols. If the board's performance becomes processor-limited by the internal 68360 processor, you can add a 68040 processor and obtain a fourfold increase in performance. $3495. **Radstone Technology Corp**, Montvale, NJ. (201) 391-2700.
Circle No. 471

Development system for TMS320C5x DSPs provides nonintrusive, full-speed emulation. The EDS320C5X expandable development system provides access to all memory and internal DSP registers. The development system connects to a PC's bidirectional printer port and obtains power either from the target system or from an external wall-mount supply. Based on a card-stacking design, the development system lets you add additional memory and other options by adding cards. The source-level debugger is compatible with Texas Instruments' C compiler and assembler. $1499. **Spectrum Digital Inc**, Sugar Land, TX. (713) 561-6952.
Circle No. 472

VME64 single-board computers feature microSPARC and microSPARC II processors. The microSPARC-based SPARC LXE/-PLUS is compatible with Sun's SPARCclassic, and the microSPARC II-based SPARC 5/64 is compatible with Sun's SPARCstation 5. Both boards offer 8 to 96 Mbytes of DRAM. Software for the boards includes Solaris 1.1, 2.3, and real-time operating systems such as VxWorks 5.1. Prices start at $5495. **Themis Computer**, Pleasanton, CA. (510) 734-0870.
Circle No. 473

Real-time multitasking kernel for R4000 Mips processor. The Nucleus PLUS kernel includes pipes, queues, and mail boxes for intertask communications. The kernel provides counting semaphores, events, and signals for intertask synchronization. The kernel costs $7495, including source code and licensing for a single product line. There are no runtime royalties. **Accelerated Technology Inc**, Mobile, AL. (205) 661-5770.
Circle No. 474

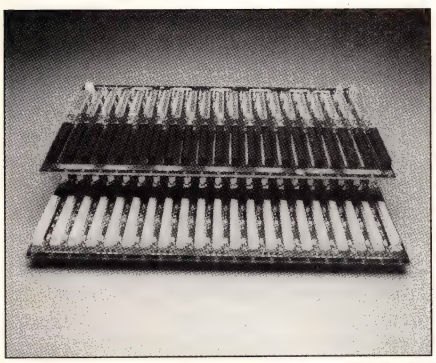
Family of VMEbus boards uses Analog Devices ADSP-21060 SHARC DSP. The 6U VMEbus boards contain one to eight DSPs and offer 120- to 960-Mflops performance. The IXZ8xxx four-processor board has three banks of global memory with a capacity of up to 256 Mbytes in each bank, two high-bandwidth I/O module connectors, eight link ports with 40-Mbyte/sec capacity. The IXZ8xxx costs less than $15,000. **Ixthos Inc**, Silver Spring, MD. (301) 572-6700.
Circle No. 475

Development system for TMS320C5x includes μP support. The Slalom-50 development system includes two 57-MHz TMS320C51 DSPs, 64k words of program memory for each DSP, 64k words of data memory for each processor, 4kx16-bit dual-port shared memory, and a source-code debugger. The development system is suitable for developing single- or dual-processor designs, shared-memory systems, time-division multiplex, and serial-port interprocessor communication schemes. $3995.

White Mountain DSP Inc, Nashua, NH. (603) 883-2430. **Circle No. 476**

Mezzanine board for VMEbus transfers data at 200 Mbytes/sec. The AutoBahn Spanceiver kit lets you create systems with high sustained data-transfer rates. The starter kit costs $4990. **PEP Modular Computers**, Scottsdale, AZ. (602) 483-7100. **Circle No. 477**

Multiband digital-receiver modules for VME and Multibus II. The modules accept 12-bit digitized data at sample rates as high as 70 Msamples/sec. Two narrowband receivers and one wideband receiver perform frequency down-conversion, lowpass filtering, and decimation of the sampled output. The modules implement conventional radio-receiver functions with digital circuits, providing a front end suitable for digital signal-processing systems. Both the VMEbus Model 4272 and the Multibus II Model 4372 start at $8995. **Pentek Inc**, Norwood, NJ. (201) 767-7100. **Circle No. 478**



Monolithic VMEbus backplanes offer automatic daisy-chain option. The monolithic backplanes improve the performance and reliability of VMEbus systems by using a common J1/J2 substrate for better impedance matching, instead of separate substrates. The backplanes meet all requirements of the VME 64 standard. Prices range from $310 for a two-slot backplane to $950 for a 21-slot backplane. **Dawn VME Products Inc**, Fremont, CA. (510) 657-4444. **Circle No. 479**

S-Bus board uses AT&T's floating-point DSP32C. The SB32C board is available with one or two processors. The single-processor version features 25-Mflops peak performance and includes one stereo codec and 512 kbytes of private SRAM. The dual-processor version features 50-Mflops peak performance and includes 512 kbytes of private SRAM for each processor and four CD-quality audio input/output channels. The single-processor SB32C1 costs $1500, and the dual-processor SB32C2 costs $2500. **Communication Automation & Control Inc**, Allentown, PA. (610) 776-6669. **Circle No. 480**

Family of ruggedized commercial and military enclosures. Open-architecture chassis systems for VME, Multibus, Futurebus+, ISA, and EISA are available. Form factors include rack-mount, ATR, hard-point and mobile mountings for industrial, shipboard, aircraft, and ground mobile applications. **AP Labs Inc**, San Diego, CA. (619) 546-8626. **Circle No. 481**

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Design tool helps FPGA vendors test and refine new architectures. The Figaro Architect's Workbench uses parameterized behavior models to test new architectures. According to the company, the tool can cut development time by as much as 50%. The tool lets FPGA vendors test architectures during the design stage against PREP benchmarks or actual customer applications. Architect's Workbench starts at $250,000. **Cadence Design Systems Inc**, San Jose, CA. (408) 943-1234. **Circle No. 394**

Simulator runs faster when using VITAL-compliant models. The V-Systems VHDL simulator now runs two to eight times faster for designs using VITAL-compliant gate-level models or primitives. V-Systems costs $2495 for use on PCs under Windows and $9995 for a floating workstation license. **Model Technology Inc**, Beaverton, OR. (503) 641-1340. **Circle No. 395**

Graphical state-machine design tool offers animation for following state transitions. BetterState Pro V2.0 lets you graphically design state machines and then automatically generates the state machine code in C, C++, Verilog, or VHDL. In addition to standard state-machine design techniques, the tool lets you use extended state diagrams with hierarchy and concurrence and multirate-firing Petri Net design-entry methods. During design, you can interactively view a series of state transitions graphically. After designing and simulating a state machine, you can use the tool's animated playback capability to view state-transition sequences. The software also computes state-visitation statistics for analyzing designs. BetterState Pro costs $495, including one code generator. Additional code generators for other languages are $99 each. **R-Active**, Cupertino, CA. (408) 252-2808. **Circle No. 396**

Design-for-test software adds IDDQ, ATPG, and scan-test improvements. FlexTest and FastScan have new algorithms for selecting a compact set of test vectors for IDDQ testing. New algorithms in DFTAdvisor help minimize area on partial-scan designs while providing higher test coverage. FastScan and FlexTest cost $92,400, and DFTAdvisor costs $20,000. **Mentor Graphics**, Wilsonville, OR. (503) 685-8000. **Circle No. 397**

Tool links corporate component database with schematic capture. PROdatabook is a PC-based component data-entry and -verification tool that links schematic capture with component databases. The tool costs $1495 for a single user and $14,995 for a site license. **Viewlogic Systems Inc**, Marlborough, MA. (508) 480-0881. **Circle No. 398**

IC power-analysis tool lets you analyze power consumption early in the design cycle. DesignPower provides both probabilistic and simulated power-analysis tools. Probabilistic power analysis is useful for evaluating power consumption during early design stages. Simulated power analysis uses switching activity of primary inputs and internal nets from a logic simulator, providing more accurate results in the later stages of gate-level design. DesignPower costs $30,000. **Synopsys Inc**, Mountain View, CA. (415) 962-5000. **Circle No. 399**

Windows-based pc-board-design tool adds on-line DRC and built-in autorouter. TangoPRO PCB version 2.5 now offers on-line design-rule checking (DRC) that helps you find and fix design problems while you design. The built-in QuickRoute maze router handles simple routing requirements. Editing features have also been improved in the new version. TangoPRO PCB costs $5950, and TangoPRO PCB Lite, a reduced-function version without on-line DRC, costs $1995. **Accel Technologies Inc**, San Diego, CA. (619) 554-1000. **Circle No. 400**

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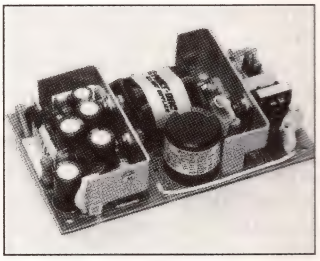
Open-frame linear supplies sport toroidal transformers. A line of open-frame linear supplies have toroidal transformers. The transformers enable these supplies to have increased efficiency, lighter weight, lower temperature ruse, less creepage distance, and lower leakage current than supplies having conventional transformers. Outputs range from 5 to 28V dc. $72.50 (25), delivery six to eight weeks. **International Power**, Oxnard, CA. (805) 981-1188. **Circle No. 401**

High-density dc/dc converters in 100 to 300W power ranges. These 100 to 300W converters accept inputs from 48 to 300V dc and provide a single output ranging from 1.2 to 15V. HDL series converters deliver full output power with baseplate temperatures as high as 85°C. HDK series converters are similar but have monitoring and control functions referenced to either the primary or the secondary. HDM series converters allow full output power at baseplate temperatures of 100°C. The converters measure 4.6×2.4×0.5 in. and have an MTBF of more than one million hours. From $137 for the HDK100 series to $299 for the HDM300 (100). **Digital Power Corp**, Fremont, CA. (510) 657-2635.
Circle No. 402

DC/DC converters available in surface-mount package. The 1W HL01 and 2W HL02 are available in 24-pin DIP and SMD packages. Up to 48 models of each type are available with input ranges from 5 to 24V dc and single or dual outputs from 5 to 15V. All devices are rated for full power at 70°C with no external heatsink. OEM pricing: $5 for the HL01; $6 for the HL02. **Burr-Brown Power Convertibles Corp**, Tucson, AZ. (602) 628- 8292.
Circle No. 403

Ruggedized dc/dc converters offer up to 200W output power. The LC810 series converters use full military fixed-frequency design and construction and meet MIL-STD-810 environments. $700 in volume. **EG&G Power Systems Inc**, Covina, CA. (818) 967-9521.
Circle No. 404



40W triple-output supply has 5V at 5A. The MAP40-3500 supply also has 12V at 1A and –12V at 0.5A. The 3×5×1.6-in. supply provides automatic ac input selection from 90 to 264V ac, onboard filtering that meets FCC and VDE Class B conducted-emission requirements, a variety of safety agencies' certification, and a two-year warranty. $49 (100). **Power-One Inc**, Camarillo, CA. (805) 987-8741. **Circle No. 405**

0.75W dc/dc converter is available in 14-pin DIP and surface-mount packages. The HPR1xx unregulated converters accept 5, 12, 15, and 24V inputs and have single or dual outputs. The converters are rated for full power operation to 85°C without heatsinks. <$5 (OEM qty). **Burr-Brown Power Convertibles Corp**, Tucson, AZ. (602) 628- 8292.
Circle No. 406

Triple-output linear power supply designed for pc-board mounting. The Model 3.15.1000 low-noise linear power supply provides ±15V at ±100 mA and 5V at 1A. Typical output noise is 2 mV rms. Line and load regulation is ±0.2% maximum, and voltage accuracy is ±1%. The supply is housed in a 3.5×2.5×1.5-in. case and has an operating temperature of –25°C to +50°C. Standard input is 115V ac, with other modules available for 100, 220, 230, and 240V ac. $115.76 (100). **Calex Mfg Co Inc**, Concord, CA. (510) 687-4411.
Circle No. 407

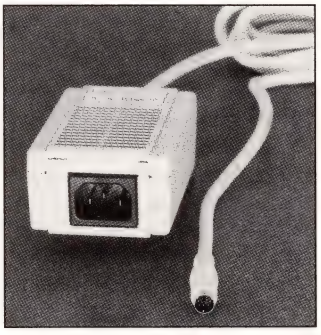
600W switcher has low profile. The series 126 switching power supply measures 5×13.5×2.5 in. and accepts inputs from 90 to 132 and 180 to 264V ac. Model 126-01 offers 5V dc at 100A, 12V dc at 20A, and –12V dc at 10A. Total supply output power is limited to 600W with 50-cfm airflow. $435 (1000). **Conversion Equipment Corp**, Orange, CA. (714) 637-2970.
Circle No. 408

5W dc/dc converter operates from –55°C to +125°C. Model 2578 converter is hermetically sealed in a 0.38×1.06×1.06-in. package. The converter operates from 28V dc with MIL-STD-704 or MIL-STD-1275 surge characteristics. Available in single-, dual-, and triple-output configurations, the converters start at $350 (10). **Modular Devices Inc**, Shirley, NY. (516) 345-3100.
Circle No. 409

Subminiature linear power supply provides 5V dc at 300 mA. The 1.75×2.26×1.0-in. model 21-30 provides a low-noise 5V output from 115V ac input (optionally 100, 220, 230, or 240V ac). The supply has current-limiting short-circuit protection, 1000V-rms isolation, and a case-operating temperature of –25°C to +50°C. $67.20. **Calex Mfg Co Inc**, Concord, CA. (510) 687-4411.
Circle No. 410

4W dc/dc converter offers high isolation for medical applications. The HB04 converter has 8000V isolation; 18 models are available with inputs ranging from 5 to 15V and single or dual outputs ranging from 5 to 15V. The converter also offers low isolation-barrier capacitance, suiting the device for driving IGBTs in motor-drive applications. <$40. **Burr-Brown Power Convertibles Corp**, Tucson, AZ. (602) 628- 8292.
Circle No. 411

Compact dc/dc converters provide bias supply voltage for LCD contrast. Packaged in SIPs, these converters accept either 4.5 to 5.5V dc or 10 to 25V dc. HN and HW models offer outputs of –22, –23, or –24V dc. The EPN series has an output adjustable from –14 to –24V dc, and the RD series' output is adjustable from 24 to 40V dc. Power ratings range from 0.5 to 1.8W. From $3.50 (OEM qty). **Xentek Inc**, San Marcos, CA. (619) 471-4001.
Circle No. 412



20W desktop power supplies available with single, dual, and triple outputs. Vulcan line switching power supplies are available in desktop versions measuring 3.9×2.5×1.5 in. This power-supply line has all major safety and EMI approvals, including medical. Outputs range from 3.3 to 24V dc. From $25 (1000). **LZR Electronics Inc**, Gaithersburg, MD. (301) 921-9440. **Circle No. 413**

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16-bit, 100k-sample/sec ADC board costs $699. The 16-channel (eight differential) CIO-DAS 1602/16 samples twice as fast as boards with which it is compatible. A 512-point FIFO buffer stores new data during DMA transfers, enabling seamless acquisition. Software-programmable gains provide 1.25, 2.5, 5, and 10V unipolar and bipolar ranges. The board also contains two 12-bit DACs, three 16-bit counters, and 32 bits of digital I/O. **Computer Boards Inc**, Mansfield, MA. (508) 261-1123. **Circle No. 452**

Windows-based tool set simplifies development of DSP applications. WinSpox speeds the development of Windows 3.1-based instrumentation, data-acquisition, and signal-analysis applications by allowing Windows software to start, stop, and communicate with DSP-resident tasks. Communication occurs via messages and streaming data. The tool set, which is based on the Windows Resource Manager Interface (RMI), is indifferent to the type of DSP chip used (although the DSP must run the vendor's Spox V2.0 DSP OS) and to whether the DSP resides on the PC's system board or on an I/O card. $3000. **Spectron Microsystems Inc**, Santa Barbara, CA. (805) 968-5100.
Circle No. 453

PLD ATPG software generates race-free vectors in minutes. FS-ATG V3.0 software uses a full circuit simulator to analyze PLDs' internal logic. Starting from the simulation, the package develops race-free vectors within minutes. By using menus, you can set the degree of fault coverage you desire, specify the maximum permissible runtime, and define the information you want presented in testability reports. The package produces vector definitions in JEDEC format. An optional translator converts these into formats suited to programmers, component testers, and in-circuit ATE. From $1900. **Flynn Systems Corp**, Nashua, NH. (603) 891-1111. **Circle No. 454**

Stand-alone IC programmer handles gangs, sets, and sets of sets up to 64 bits wide. Model 2000 takes no more time to program 16 devices than it takes to program one. It accepts 8-, 16-, 32-, and 64-bit data and works with devices having as many as 94 pins packaged in PLCCs, QFPs, TSOPs, DIPs, SOICs, and others. The unit programs, verifies, and sum-checks 1-Mbit EPROMs in 18 sec; 2-Mbit parts take 34 sec. $1995; socket modules, $995. **Bytek Corp**, Boca Raton, FL. (407) 994-3520. **Circle No. 455**

Multiproduct calibrator eases ISO 9000 registration. The 5500A calibrates digital and analog multimeters, digital and analog scopes (to 200 MHz), thermometers, power meters, harmonic analyzers, process calibrators, data loggers, current transducers, and chart recorders. The unit provides dc and ac voltages to 1 kV, dc and ac current to 11A, resistance from a short circuit to 330 MΩ, frequencies from 2 Hz to 2 MHz with multiple waveforms, and capacitance from 330 pF to >1 μF. It also simulates thermocouples and RTDs from –250 to +2310°C and dc and ac power to 11 kW. All capabilities reside in a 7-in.-high rack-mountable unit that operates by itself or with a PC. $9995; scope-calibration option, $6500; software, $2500. **Fluke Corp**, Everett, WA. (800) 443-5853.
Circle No. 456

Graphical instrument-control software works with Radisys embedded VXI controller. HP VEE for Windows, a programming system in which you write programs by interconnecting icons, now runs on Radisys Corp's EPC-7 embedded VXIbus controller. Until Nov 30, the controller with VEE for Windows factory-installed on the hard drive costs $8735—$750 less than the regular price. Also until Nov 30, either HP VEE for Windows or Data Translation Inc's DT VEE for Windows (a version of VEE that supports Data Translation's data-acquisition boards) cost $998, 50% less than the regular prices. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844.
Circle No. 457

Diagnostic tool for RS-232C or CCITT V.24 data interface. The Model 700 EIA RS-232C interface analyzer helps diagnose communication-interface problems on modems, multiplexers, terminals, and computers. The unit connects between data-terminal equipment and data-communications equipment to provide access and monitoring of all data, timing, and control signals. $195. **Electro Standards Laboratory Inc**, Cranston, RI. (401) 943-1164. **Circle No. 458**

Data-logging add-on software for LabView 3.0 provides historical trending. Fast HIST suits data logging at up to 10 samples/sec. Fast HIST and Standard HIST are bundled together in HIST 3. $250. **Gary Johnson**, Livermore, CA. (510) 606-1335.
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FFT library suits DSP and spectral-analysis-development applications Prime Factor FFT Library provides routines written in assembly language for fast execution that are callable from any language. The software computes forward and inverse FFTs of signals, allowing frequency-domain analysis of signals recorded in the time domain. Windows version, $395; DOS version, $295. **Alligator Technologies**, Costa Mesa, CA. (714) 850-9984.
Circle No. 460

ISA bus board digitizes waveforms to 12-bit resolution at 60 Msamples/sec. The DA60 board digitizes a single channel at up to 60M samples/sec or two channels at up to 30M samples/sec simultaneously. Each channel has 256k words of memory, or you can use the full 512k words when recording a single channel. Digital attenuators provide a full-scale input-voltage range of 100 mV p-p to 5V p-p with an input impedance of 50Ω. The board includes a library of C functions for developing custom applications. $4900. **Signatec Inc**, Corona, CA. (909) 734-3001.
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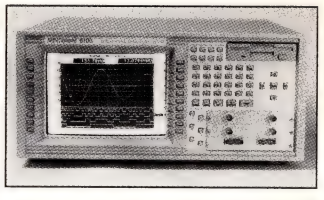

DSO has sourcing and measuring capability that lets you configure system for ATE applications. The System 8100 Series digital storage oscilloscope (DSO) has a variety of plug-in modules that let you configure the system for self-contained mixed-signal test-and-measurement applications. The basic DSO has a 100-MHz bandwidth, 100M sample/sec digitizing rate, and 100-psec timing resolution. The system captures

multiple channels of digital and analog waveforms simultaneously, depending on the plug-ins used. A built-in 3.5-in. floppy-disk drive stores waveforms. The DSO will be available in the fourth quarter. $3500. **Mint Systems Corp**, Milpitas, CA. (408) 262-7171.
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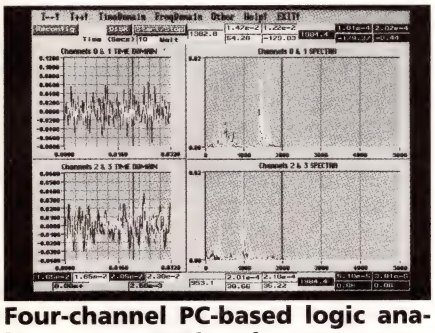
E-beam prober for advanced ICs offers 20× speed improvement. The IDS 10000 acquires detailed waveform information on advanced chips in less than 1 minute. The speed improvement results from using a thermal-field-emission column. Other prober features are a 5-mV-rms noise specification and the ability to measure ac waveforms down to 50 mV. The prober costs more than $1 million. **Schlumberger Technologies, ATE Division**, San Jose, CA. (408) 453-0123.
Circle No. 463

ISA bus and VESA local-bus extender operate at 50 MHz. The FVL/ISAext-S extender brings all 90 VESA local-bus lines and all 88 ISA bus lines to logically ordered rows of push-on test posts, which connect to any logic analyzer or any board mounted on the extender. The logical ordering of signals simplifies test-point connections instead of the confusing physical ordering of conventional extenders. The board also has test jacks that output a voltage proportional to the current drawn by the board under test. $249. **Ultraview Corp**, Fremont, CA. (510) 657-9501. **Circle No. 464**



Four-channel PC-based logic analyzer uses National Instruments data-acquisition board. The DBA PC-based spectrum analyzer software runs under DOS or Windows and uses the AT-A2150 data-acquisition board. The spectrum analyzer performs single and double integration, power-spectrum analysis, FFTs, and windowing using Hamming, Blackman, Kaiser, triangular, rectangular, and Hanning windows. Software, $1195 for DOS systems; $1495 for Windows systems. A turnkey portable-PC-based system costs $5837. **Carman Enterprises**, Loveland, OH. (513) 677-5363.
Circle No. 465

Data-acquisition and -analysis software suits real-time applications. Viewdac 2.2 works with the company's instruments and IEEE-488 and RS-232C instruments. Enhancements available in the new version include a call task that works similarly to a macro or subroutine, letting you use the same instructions more than once in the same application. An array-display task reduces the coding needed to create displays of numeric-value arrays. Added dialog boxes help you create the control lists for controlling task execution. Application Development Package, $1995; runtime license, $400. **Keithley Metrabyte**, Taunton, MA. (508) 880-3000. **Circle No. 466**

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Color X terminals break $1000 barrier. The ECX breaks the $1000 price barrier for a color X terminal system. The base electronics cost $845 for an entry-level system; adding a low-cost color PC monitor results in a total cost of <$1000. The ECX is a MC68020-based unit that you can combine with any SVGA VESA-conformant multisync monitor. **Network Computing Devices Inc**, Mountain View, CA. (415) 694-0650. **Circle No. 380**

AT-compatible workstations offer Pentium performance. The Series 400 industrial, AT-compatible workstations provide Pentium performance and a choice of flat-panel displays. The rugged systems suit industrial-operator-interface, monitoring, and control applications that have severe space constraints or high EMI. The workstations come with a 486SX/33, DX/33, or DX2/66 processor; the CPU board can also accept a 486DX4/100 or Pentium P24T. Display choices include a 10.4-in., high-brightness, monochrome, electroluminescent display or a color TFT LCD. From $5000. **Nematron Corp**, Ann Arbor, MI. (313) 994-0591. **Circle No. 381**

486-based computer works on passive backplane. The CAT1015 single-board computer for passive backplanes has processor options that include a 100-MHz 80486 DX4 in a full-size, AT expansion-card form factor. Page-mode DRAM with 8 kbytes (16 kbytes for 80486 DX4) of internal cache provides zero-wait-state performance. Up to 64 Mbytes of onboard system memory are available, accepting 256-kbyte, 1-Mbyte, or 4-Mbyte×36-bit SIMMs. $2045 without RAM. **Diversified Technology**, Jackson, MS. (601) 856-4121. **Circle No. 382**

Removable drive has 4.2-Gbyte capacity. The Mercury 4.2-Gbyte Superfast Drive (R4-420XS-ME) uses a fast SCSI-2 interface for data transfers as fast as 10 Mbps. The drive's fully sealed, static-protected enclosure provides isolastic shock absorption. With a 7200-rpm spindle speed, the drive has an average seek time of <8 msec. Additionally, the drive uses an internal 1-Mbyte cache and contains support for fault tolerance, RAID (redundant array of inexpensive disks), and network environments. $3999. **Mega Drive Systems Inc**, Beverly Hills, CA. (310) 247-0006. **Circle No. 383**

Minicartridge backup drive has 680-Mbyte capacity. The Tape510 1/4-in. cartridge (QIC)-tape backup drives store 255 Mbytes using standard tape cartridges (510 Mbytes with compression) or, with extended-length cartridges, 340 Mbytes (680 Mbytes with compression). The drive is based on the QIC 3010 minicartridge standard and reads QIC-40 and -80 and Irwin-formatted tapes. The $399 Tape510 Internal plugs into a floppy-disk controller. The $599 Tape510 parallel port uses an IEEE 1284 parallel port. **IOmega Corp**, Roy, UT. (801) 778-1000. **Circle No. 384**

PCMCIA fax/modem card operates at 28.8 kbps. The ST288VFC V.FAST-compatible PCMCIA fax/modem card operates at 28.8 kbps for data and 14.4 kbps for fax. With V.42bis data compression, throughput is equivalent to 115.2 kbps. An ultra-low-power sleep mode extends battery life in mobile applications. The cards comply with V.42 and V.42bis CCITT standards. Phone-line circuitry is built into the card, which comes with a telephone cable. $499. **Smart Modular Technologies**, Fremont, CA. (510) 623-1231. **Circle No. 385**

PCMCIA SCSI card features plug-and-play and hot-swapping. The 16-bit RT7000 PCMCIA SCSI card is compatible with most SCSI peripherals and operates in any PCMCIA I type II or III slot. Plug-and-play capability and autoconfiguration make the card easy to install, according to the vendor. The card includes peripheral support for SCSI devices and comes with a 33-pin PCMCIA to 50-pin high-density SCSI-2 cable. $220. **Rancho Technology Inc**, Rancho Cucamonga, CA. (909) 987-3966. **Circle No. 386**

DSP card has CD-quality audio. The Ambassador DSP-based audio card adds CD-quality audio to the Spectrum Envoy line of telephony board products. Based on IBM's MDS2780 chip, the card has 16-bit stereo sound, CD-ROM interface, Sound Blaster compatibility, and plug-and-play installation. $100 (OEM). **Spectrum Signal Processing Inc**, Burnaby, BC, Canada. (604) 421-5422.
Circle No.387

Quadruple-speed CD-ROM recorder makes CDs in 15 minutes. The CDR4x CD-ROM recorder is a half-height SCSI unit that installs either inside or outside computer systems. PC and Macintosh configurations cost $5995 and include DiscMaker premastering and mastering software. Unix configurations cost $7495. **DataDisc Inc**, Gainesville, VA. (703) 347-2111. **Circle No. 388**

Adapter lets you run a Type III PCMCIA device in a Type I or II slot. All PCMCIA card devices that conform to the Type III specification, such as hard drives and global positioning systems, may be used with the adapter. $49. **Greystone Peripherals Inc**, Los Gatos, CA. (408) 866-4739. **Circle No. 389**

Flash memory cards offer execute-in-place system operation. The 2- to 10-Mbyte PCMCIA memory cards from Hitachi provide execute-in-place (XIP), an application program stored in the flash card that is executed directly from the card instead of being loaded into RAM. According to the company, this approach produces a smaller, faster, and more rugged system that operates longer on batteries. The 250-nsec, 2-Mbyte HB286116C-25 costs $230 (500). **Hitachi America Ltd, Semiconductor & IC Division**, Brisbane, CA. (800) 285-1601, ext 16.
Circle No. 390

PCMCIA interface is available for the Sun SPARCstation. The S-Bus card accepts up to two Type II PCMCIA cards or one Type III PCMCIA card. $295. **Sun Microsystems Computer Corp**, Mountain View, CA. (800) 821- 4643.
Circle No. 391

PCMCIA-compliant card bay for PCI-local bus-based desktop computers. CardBay-PCI is an internal PC-card bay that allows PCI-based desktop computers to add up to four sockets for PCMCIA 2.0+ Type I, II, and III cards. The card bay may be used with a variety of PCMCIA cards, including SRAM, flash, I/O, hard-disk drive, and communications. The unit includes an onboard speaker for fax/modem applications and is designed for use with DOS 3.3 or Windows 3.0 or above operating systems. $105 (100). **Cardwell International Corp**, Folsom, CA. (916) 985-1880.
Circle No. 392

Keyboards may be programmed to make any key a macro key. The Maxi Pro-II is a 124-key keyboard that lets you remap any key or use keys as macro keys to perform multikey functions. A utility included with the keyboard lets you display an image of the keyboard directly on the computer screen. The utility highlights any keys that have been remapped or are macros and shows their functions. $40 (100). **Maxi Switch Inc**, Tucson, AZ. (602) 294-5450.
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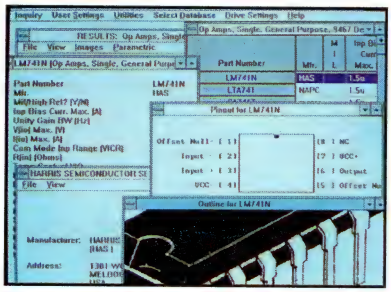

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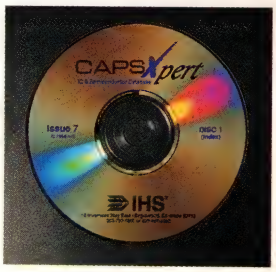

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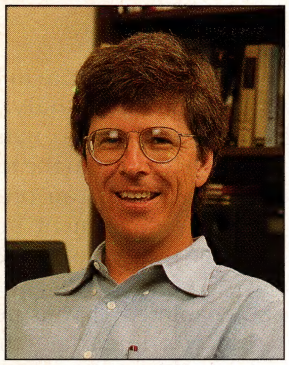

JACK GANSSLE,
EMBEDDED-SYSTEMS
CONTRIBUTING EDITOR

Troubleshooting

Avoiding the bog

There comes a time in any project when your new design is finally assembled, awaiting your special expertise to "make it work." Sometimes, it seems like the design end of this business is the easy part; troubleshooting prototype hardware can make even the toughest engineer a Maalox addict.

You can't fix any embedded system without the right world view—suspicion tempered with trust in the laws of physics, curiosity dulled only by the determination to stay focused on a single problem, and a zealot's regard for the scientific method.

Perhaps these are successful characteristics of all who pursue the truth. In a world that surrounds us with complexity, we deal daily with equipment and systems we only half understand. So, it seems wise to follow understanding by an iterative loop of focus, hypothesis, and experiment.

Too many engineers fall in love with their creations, only to be continually blindsided by the design's faults. They are quick to assume, overtly or subconsciously, that the problem is due to the software, the lousy chips, or the power company, when simple experience teaches us that any new design is rife with bugs.

Assume it's broken. Never figure anything is working right until proven by repeated experiment; even then, continue to view with suspicion the "fact" that it seems to work. Bugs are not bad; they're merely a test of your troubleshooting ability.

Armed with a healthy skeptical attitude, the basic philosophy of debugging any system is to complete the following steps:

```
For (i=0; i< # findable bugs; i++)
  {
  while (bug(i))
    {
    Observe the behavior to find the apparent bug;
    Observe collateral behavior to gain as much information as possible about the bug;
    Round up the usual suspects;
    Generate a hypothesis;
    Generate an experiment to test the hypothesis;
    Fix the bug;
    };
  };
```

Now, you're ready to start troubleshooting, right? Wrong! Stop a minute and make sure you have good access to the system. No matter how minor the problem seems to be, troubleshooting is like a bog where we all get trapped for far too long. Take a minute to ease your access to the system.

Do you have extender cards if they're needed to scope any point on the boards? How about special long cables to reach the boards once they are extended?

If there's no convenient point to *reliably* scope on the scope's ground lead, solder a resistor lead onto the board, so that you're not fumbling with leads that keep popping off.

Some systems have signals that regulate major operating modes. Solder a resistor lead on these points as well, because you'll need to scope them at some point. This small investment in time up front will pay off in spades later.

Following the loop

Let's cover each step of the troubleshooting sequence in detail:

Step 1: Observe the behavior to find the apparent bug. In other words, determine the bug's symptoms. Remember that many problems are subtle and exhibit themselves via a confusing set of symptoms. The fact that the first digit of the LCD fails to display may not be a useful symptom — but the fact that none of the digits work may mean a lot.

Step 2: Observe collateral behavior to gain as much information as possible about the bug. For example, does the LCD's problem correlate to a relay's clicking in? Avoid studying a bug in isolation but beware of trying to fix too many bugs at once. Address such problems as ROM accesses' unreliability and a not-bright-enough front-panel display one at a time. No one is smart enough to deal with multiple bugs all at once, unless they are all manifestations of something more fundamental.

Step 3: Round up the usual suspects. In other words, many computer problems stem from the same few sources. Clocks must be stable and meet specific timing and electrical specs, or all bets are off. Reset too often has unusual timing parameters. When things are just "weird," take a minute to scope all critical inputs to the µP, such as clock, hold, ready, and reset.

Always remember to check V_{cc}. Time and

PHOTOGRAPHY / HOWARD DAVIS

time again at Softaid, we see systems that don't run right because the 5V supply is putting out only 4.5 or 5.6V, or 5V with lots of ripple. The systems come in after their designers have spent weeks sweating over some obscure problem that, in fact, never existed, but was simply the specter of the more profound power-supply issue.

Step 4: Generate a hypothesis. Don't be like "shotgunners," those poor fools who address problems by simply changing things—ICs, designs, PLD equations—without having a rationale for the changes. Shotgunning is for amateurs. It has no place in a professional engineering lab.

Before changing things, formulate a hypothesis about the cause of the bug. You probably don't have the information to do this without gathering more data. Use a scope, an emulator, or logic analyzer to see exactly what *is* going on; compare that with what you think *should* happen. Generate a theory about the cause of the bug from the difference in these.

Sometimes, you have no clue to what the problem is. Scoping the logical places might not generate much information. Or, a grand failure, such as an inability to boot, occurs that is so systemic that it's hard to tell where to start looking. When desperation sets in, it's worthwhile to scope around the board practically at random. You might find a floating line, an unconnected ground pin, or something unexpected. Scope around, but always be on the prowl for a working hypothesis.

Step 5: Generate an experiment to test the hypothesis. Most of the time, you can resolve this step when gathering data to come up with the theory in the first place. For example, if an emulator reads all ones from a programmed ROM, a reasonable hypothesis is that CS or OE isn't toggling. Scoping the pins proves this one way or the other, but requires you to formulate another hypothesis and experiment to figure out why the selects are not where you expect to see them.

Sometimes, though, you should apply the hypothesis-experiment model more formally. When we first started to use Intel's XL version of the 186 (supposedly compatible with the older series), none of our systems worked. Scoping around showed the processor to be stuck in a weird tristate, although all of its inputs seemed reasonable. One hypothesis was that the 186XL was not properly coming out of reset, a hard thing to capture because reset is basically a nonscopable, one-time event. We finally built a system to reset the processor repeatedly, giving us something to scope. The experiment proved the hypothesis, and a fix was easy to design.

It's much faster to think out the change than to implement it and perhaps troubleshoot it over again.

An alternative would have been to glue in a new reset circuit at the beginning to see if the problem would go away. Problems that mysteriously go away tend to mysteriously come back; unless you can prove that the change *really* fixed the problem, there may still be a time bomb lurking in the system.

Occasionally, a bug is too complicated to yield to such casual troubleshooting. If you have to adjust the timing of a PLD, visualize or draw the new timing before wildly making changes. Will it work? It's much faster to think out the change than to implement it and perhaps troubleshoot it over again.

Rapid troubleshooting is as important as accurate troubleshooting. Decide what your experiment will be and then stop and think it through again. What will this test prove? I like experiments with binary results: The signal is there, or it isn't; the signal meets specified timing, or it doesn't. Either result gives me a direction in which to proceed. Binary results have another benefit: They sometimes let you skip the experiment altogether. Always think through the actions you'll take *after* the experiment is complete, because sometimes you find yourself taking the same path, regardless of the result, making the experiment superfluous.

If the experiment is a nuisance to set up, is there a simpler approach? Hooking up 50 logic-analyzer probes is rather painful if you can get the same information in an easier way. I'd hate to b in a lab without a logic analyze because they're useful for so man things, but I try to relegate it to the too of last resort, because you can ofte construct an easier experiment in fraction of the time it takes to connec the logic analyzer.

Don't be so enamored of your ne hypothesis that you miss data tha might disprove it. The purpose of hypothesis is simply to crystallize you thinking: If it's right, you'll know th step to take next. If it's wrong, collect more data to formulate yet another theory.

Step 6: Fix the bug. There's more than one way to fix a problem. Hanging a capacitor on a PLD output to skew it a few nanoseconds is one way; another is to adjust the design to avoid the race condition entirely.

Sometimes, a quick and dirty fix might be worthwhile to avoid getting hung up on one little point. Revisit the kludge and re-engineer it properly. Electronics have an unfortunate tendency to work in the engineering lab and not go wrong until the 5000th unit is built. If a fix feels bad, or if you have to furtively look over your shoulder and glue it in when no one is looking, then it's bad.

Finally, never fix the bug and assume it's OK because the symptom has disappeared. Apply a little common sense and scope the signals to make sure you haven't fixed the problem by creating a new one.

Some final advice

At 3:00 am, when the problems seem intractable and you're ready to give up engineering, remember that the system is only a computer. Never panic: You are smarter than it is.

Jack Ganssle is the president of Softaid, a vendor of emulators and other embedded-systems tools. His idea of heaven is sailing across oceans, although the ugly face of common sense precludes these dreams too often. He can be contacted via Compuserve at "76366,3333," or via Internet at "76366.3333@compuserve.com." For those users of the Pony Express, send mail c/o Softaid, 8310 Guilford Rd, Columbia, MD 21046.

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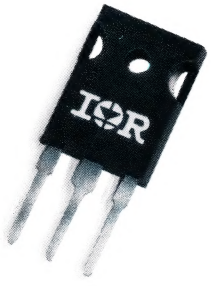

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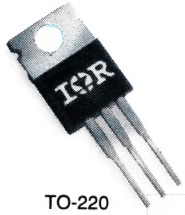

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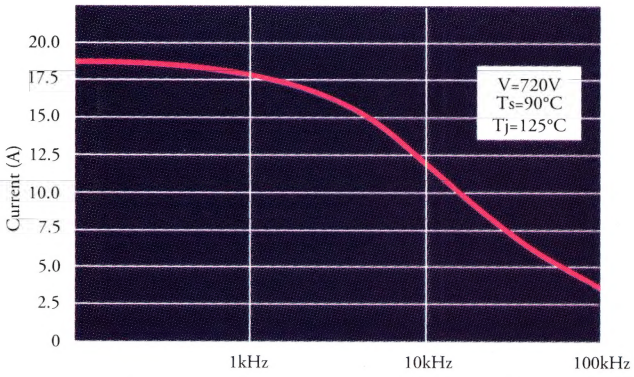

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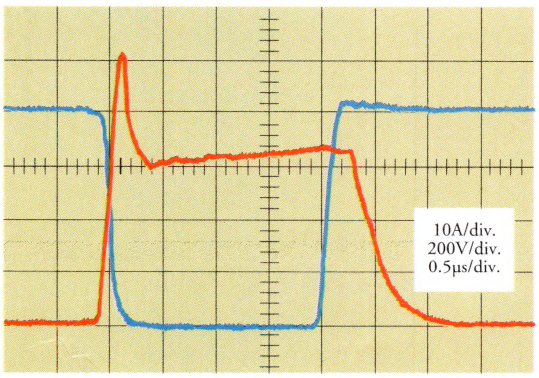

Switching waveforms of the IRGPH50KD2 in a clamped inductive load at Tj = 90°C.

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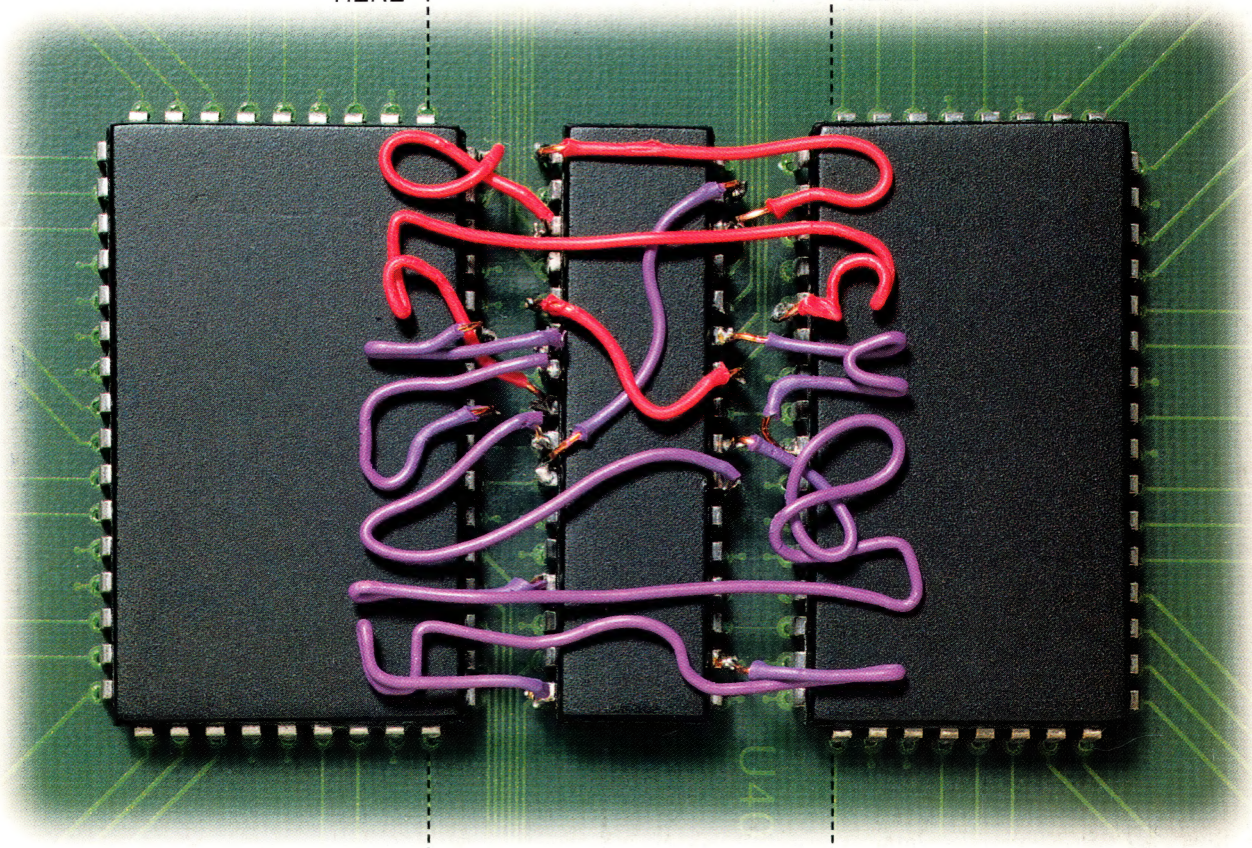

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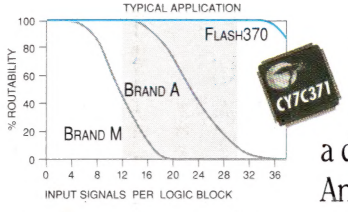

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